BASLER A102f

USER'S MANUAL

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For customers in the U.S.A.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

You are cautioned that any changes or modifications not expressly approved in this manual could void your authority to operate this equipment.

The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a computing device pursuant to Subpart J of Part 15 of FCC Rules.

For customers in Canada

This apparatus complies with the Class A limits for radio noise emissions set out in Radio Interference Regulations.

Pour utilisateurs au Canada

Cet appareil est conforme aux normes Classe A pour bruits radioélectriques, spécifiées dans le Règlement sur le brouillage radioélectrique.

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Basler customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Basler for any damages resulting from such improper use or sale.

Warranty Note

Do not open the housing of the camera. The warranty becomes void if the housing is opened.

Contacting Basler Support Worldwide

Europe:

Basler AG
Ander Strusbek 60 - 62
22926 Ahrensburg
Germany

Tel.: +49-4102-463-515
Fax.: +49-4102-463-599

bc.support.europe@baslerweb.com

Americas:

Basler, Inc.
855 Springdale Drive, Suite 203
Exton, PA 19341
U.S.A.

Tel.: +1-610-280-0171
Fax.: +1-610-280-7608

bc.support.usa@baslerweb.com

Asia:

Basler Asia Pte. Ltd.
8 Boon Lay Way
03 - 03 Tradehub 21
Singapore 609964

Tel.: +65-6425-0472
Fax.: +65-6425-0473

bc.support.asia@baslerweb.com

www.baslerweb.com

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1 Introduction

1.1 Documentation Applicability

This User's Manual applies to **A102f** monochrome cameras with a firmware ID number of 31 or **A102fc** color cameras with a firmware ID number of 34.

Cameras with a lower or a higher firmware ID number may have fewer features or have more features than described in this manual. Features on cameras with a lower or a higher firmware ID number may not operate exactly as described in this manual.

An easy way to see the firmware ID number for an **A102f** or **A102fc** camera is by using the BCAM Viewer included with the Basler BCAM 1394 driver. To see the firmware ID number:

1. Attach your camera to a computer equipped with the BCAM 1394 driver.
2. Double click the BCAM Viewer icon on your desktop or click Start ⇒ All Programs ⇒ Basler Vision Technologies ⇒ BCAM 1394 ⇒ BCAM Viewer. The viewer program window will open.
3. Find the camera name in the Bus Viewer panel that appears on the left side of the window and click on the camera name.
4. Click on the  icon in the tool bar at the top of the window.
5. A properties window similar to the one shown in Figure 1-1 will open. Use the figure as a guide to find the firmware ID number.

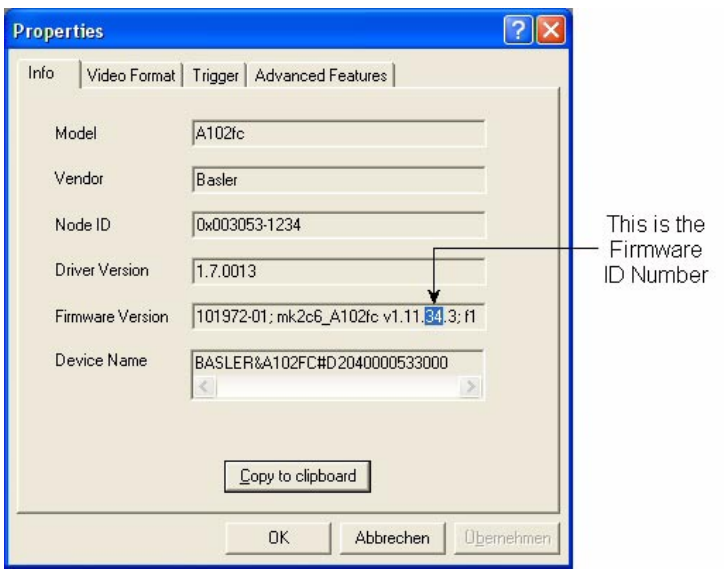

Figure 1-1: BCAM Properties Window

ⓘ	You can also access the firmware ID number by using the Extended Version Information smart feature. See Section 6.7.7 for more information.

1.2 Performance Specifications

Specification	A102f	A102fc
Sensor Type	Sony ICX-285 Progressive Scan CCD Sensor	
Pixels	1392 (H) × 1040 (V)	1388 (H) x 1038 (V)
Pixel Size	6.45 µm (H) × 6.45 µm (V)	
Mono / Color	Mono	Color
Anti-blooming	Yes	
Max. Frame Rate (at full resolution)	15.1 frames/s (in 8 bit output modes) 11.3 frames/s (in 16 bit output modes)	
Video Output Formats	Mono 8, 8 bits/pixel Mono 16, 16 bits per pixel (12 bits effective)	Mono 8, 8 bits/pixel Raw 8, 8 bits/pixel Raw 16, 16 bits/pixel (12 bits effective) YUV 4:2:2, 16 bits/pixel average
Gain and Brightness	Programmable via IEEE 1394 bus	
Exposure Time Control	Programmable via IEEE 1394 bus	
Synchronization	External via External Trigger signal	
Power Requirements	+8.0 to +36.0 VDC (+12 VDC nominal), < 1% ripple 3.5 W max @ 12 VDC supplied via 1394 cable	
I/O Electrical Characteristics	Inputs: opto-isolated, 5 VDC nominal, 10 mA nominal Outputs: opto-isolated, 2 to 35 VDC maximum forward voltage, 100 mA max collector current (See Sections 2.5.1 and 2.5.2 for more details.)	
Max. Cable Lengths	1394: 4.5 m I/O: 10 m (See Section 2.2 for more details.)	
Lens Adapter	C-mount	
Housing Size (L x W x H)	without lens adapter: 31.5 mm x 62 mm x 62 mm with c-mount adapter: 67.3 mm x 62 mm x 62 mm	
Weight	~ 240 g	
Conformity	CE, FCC	

Table 1-1: **A102f** Performance Specifications

1.3 Camera Models

The camera is available in a monochrome model (the **A102f**) and a color model (the **A102fc**). Throughout the manual, the camera will be called the **A102f**. Passages that are only valid for a specific model will be so indicated.

1.4 Spectral Response

The spectral response for the **A102f** monochrome cameras is shown in Figure 1-2.

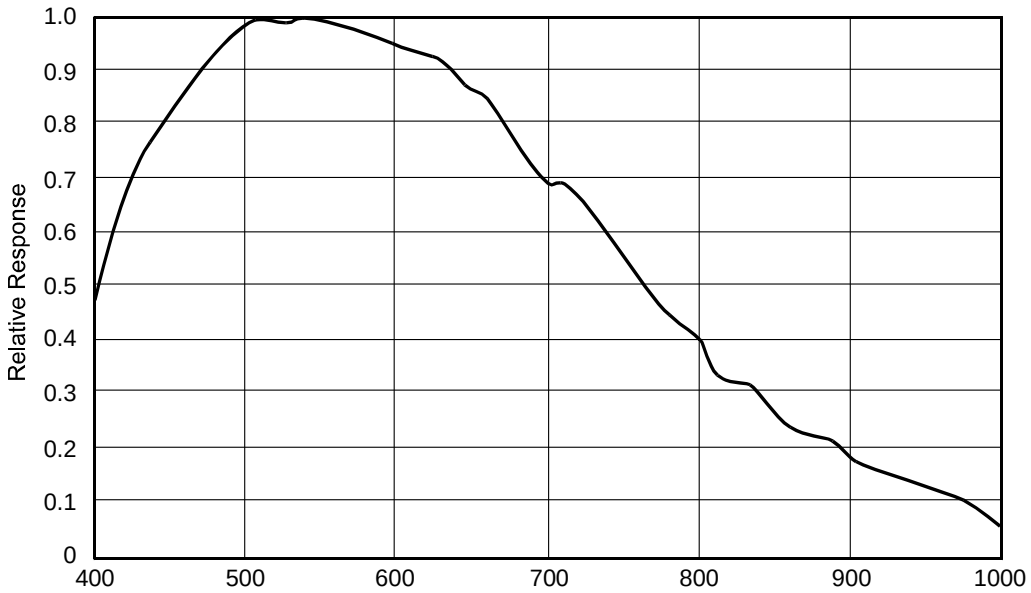

Figure 1-2: **A102f** Spectral Response - Monochrome Cameras

ⓘ	The spectral response curve excludes lens characteristics and light source characteristics.

The spectral response for **A102fc** color cameras is shown in Figure 1-3.

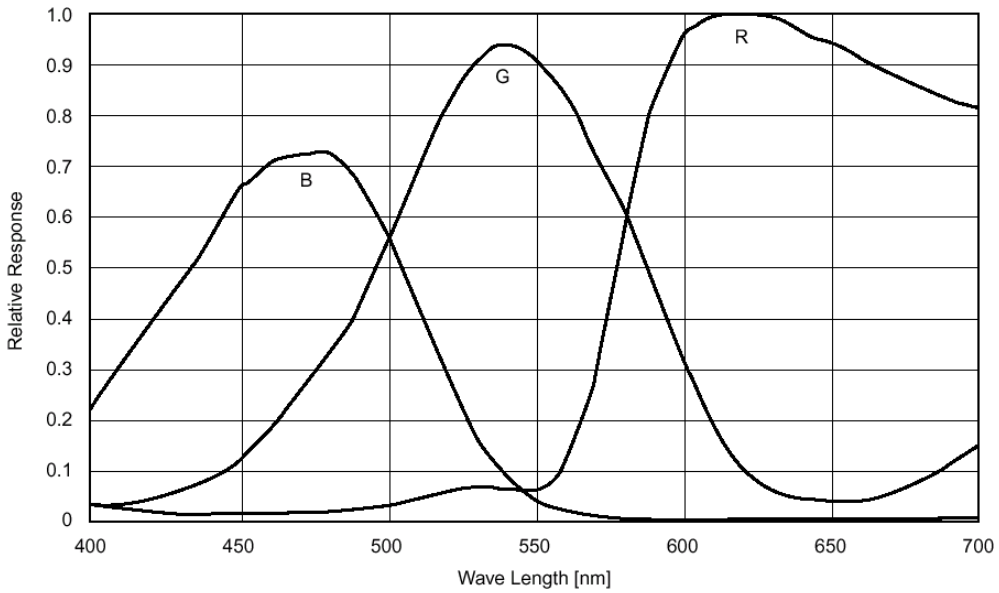

Figure 1-3: **A102f** Spectral Response - Color Cameras

	The spectral response curves exclude lens characteristics and light source characteristics. To get the best performance from **A102fc** color cameras, use of a dielectric IR cut-off filter is recommended. The filter should transmit in a range of 400 nm to 700...720 nm, and it should cut off from 700...720 nm to 1100 nm. A suitable filter is included in the standard C-mount adapter on **A102fc** cameras.

1.5 Environmental Requirements

1.5.1 Temperature and Humidity

Housing temperature during operation:	0° C ... + 50° C (+ 32° F ... + 122° F)
Humidity during operation:	20% ... 80%, relative, non-condensing

1.5.2 Ventilation

Allow sufficient air circulation around the camera to prevent internal heat build-up in your system and to keep the camera housing temperature during operation below 50° C. Provide additional cooling such as fans or heat sinks if necessary.

1.6 Precautions

To ensure that your warranty remains in force:

Read the manual

Read the manual carefully before using the camera!

Keep foreign matter outside of the camera

Do not open the casing. Touching internal components may damage them.

Be careful not to allow liquid, flammable, or metallic material inside the camera housing. If operated with any foreign matter inside, the camera may fail or cause a fire.

Electromagnetic Fields

Do not operate the camera in the vicinity of strong electromagnetic fields. Avoid electrostatic charging.

Transporting

Transport the camera in its original packaging only. Do not discard the packaging.

Cleaning

Avoid cleaning the surface of the CCD sensor if possible. If you must clean it, use a soft, lint free cloth dampened with a small quantity of high quality window cleaner. Because electrostatic discharge can damage the CCD sensor, you must use a cloth that will not generate static during cleaning (cotton is a good choice).

To clean the surface of the camera housing, use a soft, dry cloth. To remove severe stains, use a soft cloth dampened with a small quantity of neutral detergent, then wipe dry.

Do not use volatile solvents such as benzine and thinners; they can damage the surface finish.

1.7 Obtaining an RMA Number

Whenever you want to return material to Basler, you must request a Return Material Authorization (RMA) number before sending it back. The RMA number **must** be stated in your delivery documents when you ship your material to us! Please be aware that if you return material without an RMA number, we reserve the right to reject the material.

You can find detailed information about how to obtain an RMA number on the Basler website at:
www.baslerweb.com/beitraege/beitrag_en_79701.html

2 Camera Interface

2.1 Connections

2.1.1 General Description

The **A102f** is interfaced to external circuitry via an IEEE 1394 socket and a 10 pin RJ-45 jack located on the back of the housing. Figure 2-1 shows the location of the two connectors.

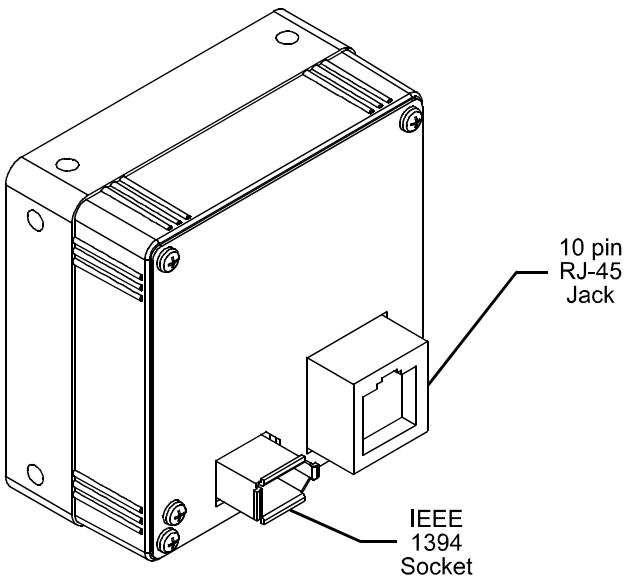

Figure 2-1: Camera Connectors

2.1.2 Pin Assignments

The IEEE 1394 socket is used to supply power to the camera and to interface video data and control signals. The pin assignments for the socket are shown in Table 2-1.

Pin	Signal
1	Power Input (+8.0 to +36.0 VDC)
2	DC Gnd
3	TPB -
4	TPB +
5	TPA -
6	TPA +

Table 2-1: Pin Assignments for the IEEE 1394 Socket

The RJ-45 jack is used to access the four physical input ports and four physical output ports on the camera. The pin assignments for the jack are shown in Table 2-2.

Pin	Designation
1	Output Port 3 -
2	Output Port 2 -
3	Output Port 1-
4	Output Port 0 -
5	Input Port 0 +
6	In Gnd Comm
7	Out VCC Comm
8	Input Port 2 +
9	Input Port 1 +
10	Input Port 3 +

Table 2-2: Pin Assignments for the RJ-45 jack

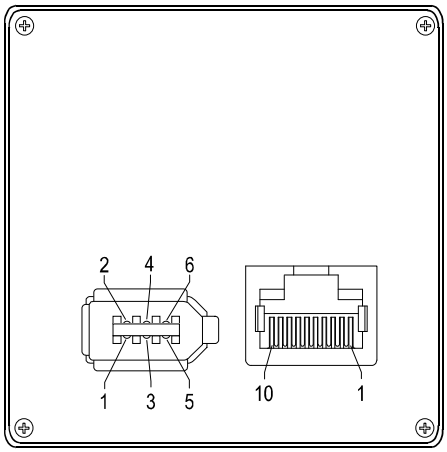

Figure 2-2: **A102f** Pin Numbering

The camera housing is connected to the cable shields and coupled to signal ground through an RC network (see Figure 2-3 for more details).

2.1.3 Connector Types

The 6-pin connector on the camera is a standard IEEE-1394 socket.

The 10-pin connector on the camera is an RJ-45 jack.

Caution!

The plug on the cable that you attach to the camera's RJ-45 jack must have 10 pins. Use of a smaller plug, such as one with 8 pins or 4 pins, can damage the pins in the RJ-45 jack on the camera.

2.2 Cables

The maximum length of the IEEE 1394 cable used between the camera and the adapter in your PC or between the camera and a 1394 hub is 4.5 meters as specified in the IEEE 1394 standard. Standard, shielded IEEE 1394 cables must be used.

The maximum length of the I/O cable is at least 10 meters. The cable must be shielded and must be constructed with twisted pair wire. Close proximity to strong magnetic fields should be avoided.

2.3 Camera Power

Power must be supplied to the camera via the IEEE 1394 cable. Nominal input voltage is +12.0 VDC, however, the camera will operate properly on any input voltage from +8.0 VDC to +36.0 VDC as specified in the IEEE 1394 standard. Maximum power consumption for the **A102f** is 3.5 W at 12 VDC. Ripple must be less than 1%.

Caution!

Use only standard IEEE 1394 connectors.

The polarity of the input power to the camera must be as shown in Table 2-1. **Do not** reverse the input power polarity. Reversing the polarity will damage the camera.

2.4 IEEE 1394 Device Information

The **A102f** uses an IEEE 1394a - 2000 compliant physical layer device to transmit pixel data. Detailed spec sheets for devices of this type are available at the Texas Instruments web site (www.ti.com).

2.5 Input and Output Ports

2.5.1 Input Ports

A102f cameras are equipped with four physical input ports designated as Input Port 0, Input Port 1, Input Port 2, and Input Port 3. The input ports are accessed via the 10 pin RJ-45 jack on the back of the camera. See Table 2-2 and Figure 2-2 for input port pin assignments and pin numbering.

As shown in the schematic in Figure 2-3, each input port is opto-isolated. The nominal input voltage for the LED in the opto-coupler is 5.0 V (± 1.0 V). The input current for the LED is 5 to 15 mA with 10 mA recommended.

For each input port, a current between 5 and 15 mA means a logical one. A current of less than 0.1 mA means a logical zero.

By default, Input Port 0 is assigned to receive an external trigger (ExTrig) signal that can be used to control the start of exposure. For more information about the ExTrig signal and for information on assigning the ExTrig signal to a different input port, see Section 3.2.5.

As stated above, the nominal input voltage for the LED on each input is +5 VDC. If a 560 Ohm resistor is added to the positive line for an input, the input voltage can be 12 VDC. If a 1.2 or 1.5 kOhm resistor is added to the positive line for an input, the input voltage can be 24 VDC.

2.5.2 Output Ports

A102f cameras are equipped with four physical output ports designated as Output Port 0, Output Port 1, Output Port 2, and Output Port 3. The output ports are accessed via the 10 pin RJ-45 jack on the back of the camera. See Table 2-2 and Figure 2-2 for output port pin assignments and pin numbering.

As shown in the schematic in Figure 2-3, each output port is opto-isolated. The minimum forward voltage is 2 V, the maximum forward voltage is 35 V, the maximum reverse voltage is 6 V, and the maximum collector current is 100 mA.

A conducting transistor means a logical one and a non-conducting transistor means a logical zero.

By default, Output Port 0 is assigned to transmit an integration enabled (IntEn) signal that indicates when exposure is taking place. For more information about the IntEn signal, see Section 3.4.

By default, Output Port 1 is assigned to transmit a trigger ready (TrigRdy) signal that goes high to indicate the earliest point at which exposure start for the next frame can be triggered. For more information about the TrigRdy signal, see Section 3.3.

The assignment of camera output signals to physical output ports can be changed by the user. See Section 6.7.11 for more information about configuring output ports.

By default, output ports 0, 1, and 2 are set to a low state after power on. Output port 3 is initially set to low but will go high approximately 100 to 300 ms after power on. Output port 3 will remain high for approximately 750 ms and will then reset to low.

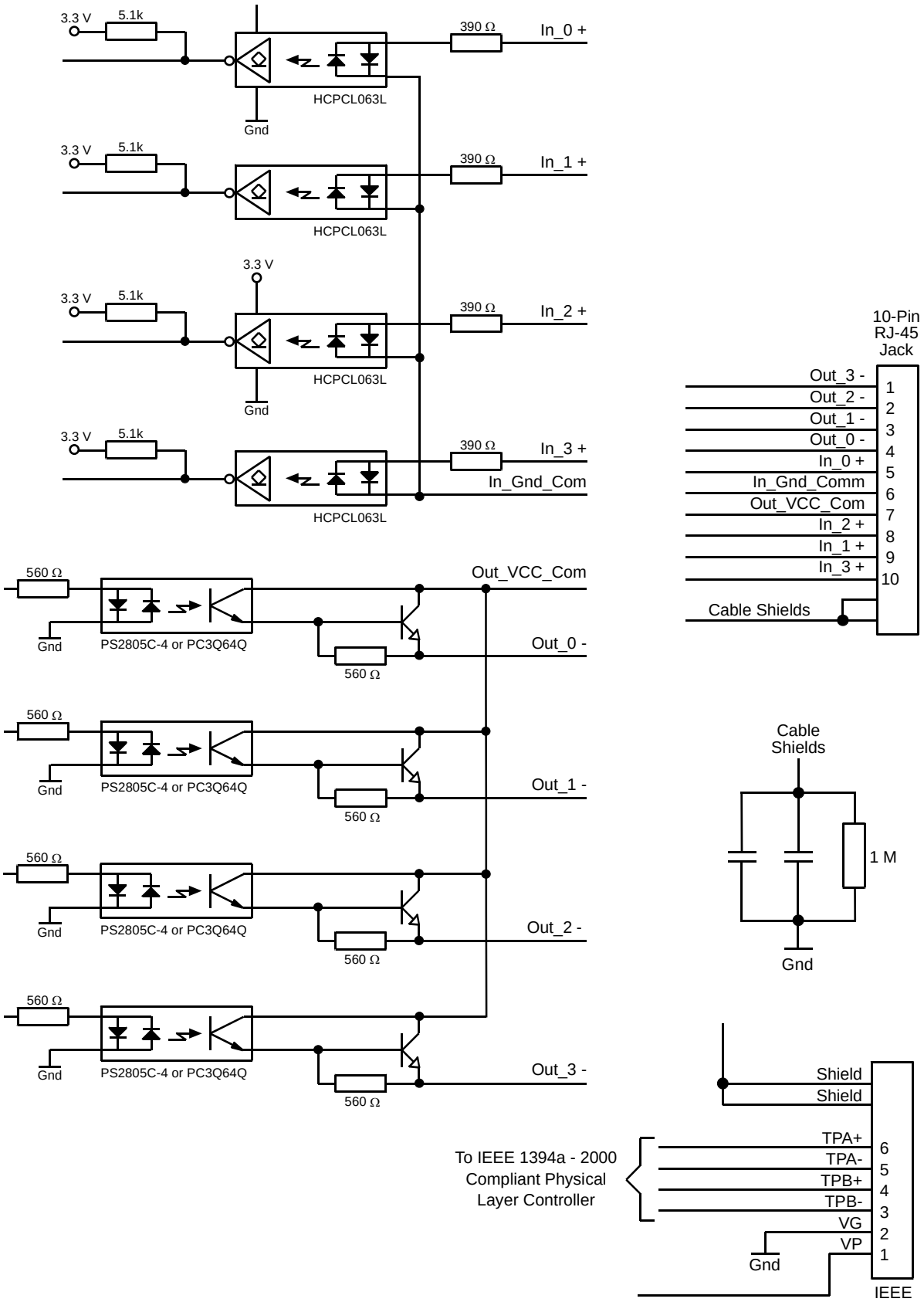

Figure 2-3: I/O Schematic

2.5.3 Typical Input Circuits

Figure 2-4 shows a typical 5 VDC circuit you can use to input a signal into the camera. In Figure 2-4, the signal is applied to input port 1.

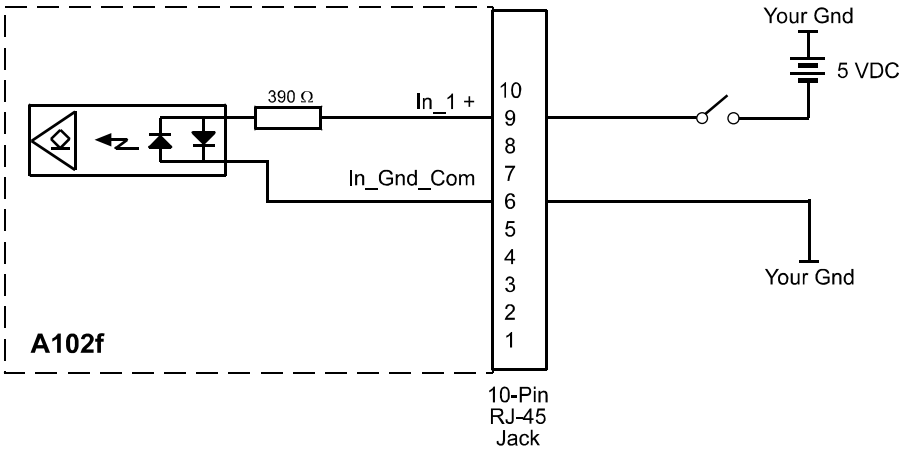

Figure 2-4: Typical 5 VDC Input Circuit

Figure 2-5 shows a typical 24 VDC circuit you can use to input a signal into the camera. Notice that an external 1.2 k resistor has been added to the circuit. This will result in approximately 15 mA being applied to the input. In Figure 2-5, the signal is applied to input port 3.

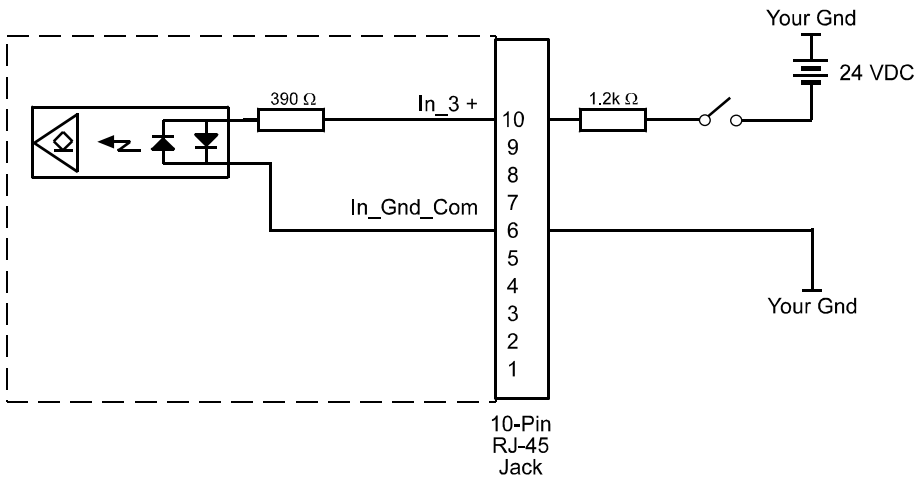

Figure 2-5: Typical 24 VDC Input Circuit

2.5.4 Typical Output Circuits

Figure 2-6 shows a typical circuit you can use to monitor an output port with a voltage signal. The circuit in Figure 2-6 is monitoring camera output port 1.

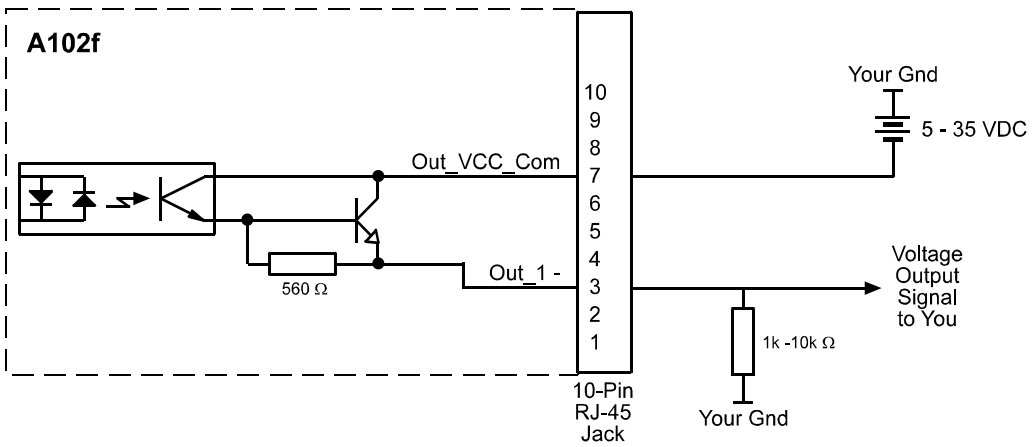

Figure 2-6: Typical Voltage Output Circuit

Figure 2-7 shows a typical circuit you can use to monitor an output port with a LED or an optocoupler. In this example, the voltage for the external circuit is 24 VDC. Current in the circuit is limited to approximately 10 mA by an external 2.2k resistor. The circuit in Figure 2-7 is monitoring camera output port 2.

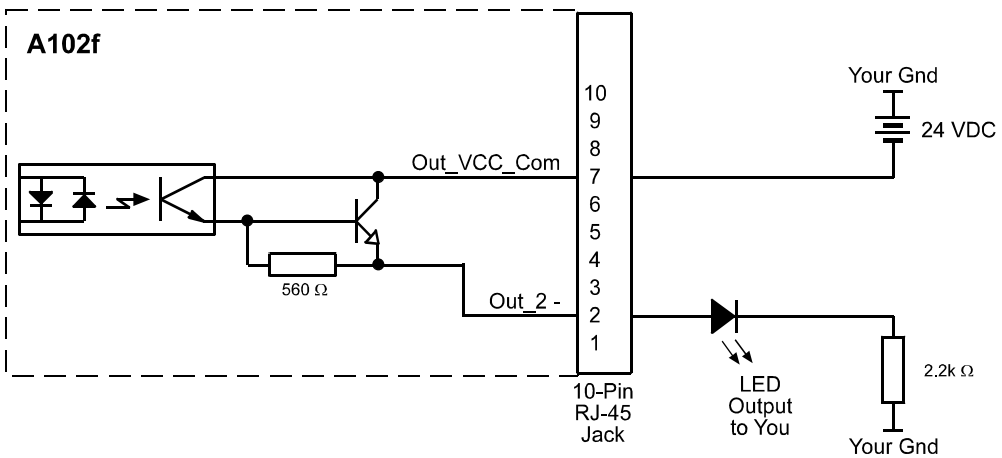

Figure 2-7: Typical LED Output Signal

3 Basic Operation and Standard Features

3.1 Functional Description

3.1.1 Overview

A102f area scan cameras employ a CCD sensor chip which provides features such as a full frame shutter and electronic exposure time control.

Normally, exposure time and charge readout are controlled by values transmitted to the camera's control registers via the IEEE 1394 interface. Control registers are available to set exposure time and frame rate. There are also control registers available to set the camera for single frame capture or continuous frame capture.

Exposure start can also be controlled via an externally generated trigger (ExTrig) signal. The ExTrig signal facilitates periodic or non-periodic start of exposure. When exposure start is controlled by a rising ExTrig signal and the camera is set for the programmable exposure mode, exposure begins when the trigger signal goes high and continues for a pre-programmed period of time. Accumulated charges are read out when the programmed exposure time ends.

At readout, accumulated charges are transported from the sensor's light-sensitive elements (pixels) to the vertical shift registers (see Figure 3-1). The charges from the bottom line of pixels in the array are then moved into a horizontal shift register. Next, the charges are shifted out of the horizontal register through an FPGA and into an image buffer. Shifting is clocked according to the camera's internal data rate.

As the charges move out of the horizontal shift register, they are converted to voltages which are proportional to the size of each charge. The voltages are amplified by an internal Variable Gain Control (VGC) and then digitized by a 12 bit, Analog-to-Digital converter (ADC). For optimal digitization, gain and brightness can be programmed by setting command registers in the camera.

The data leaves the image buffer and passes back through the FPGA to a 1394 link layer controller where it is assembled into data packets that comply with the "1394 - based Digital Camera Specification" (DCAM) issued by the 1394 Trade Association. The packets are passed to a 1394 physical layer controller which transmits them isochronously to a 1394 interface board in the host PC. The physical and link layer controllers also handle transmission and receipt of asynchronous data such as programming commands.

The image buffer between the sensor and the link layer controller allows data to be read out of the sensor at a rate that is independent of the data transmission rate between the camera and the host computer. This ensures that the data transmission rate has no influence on image quality.

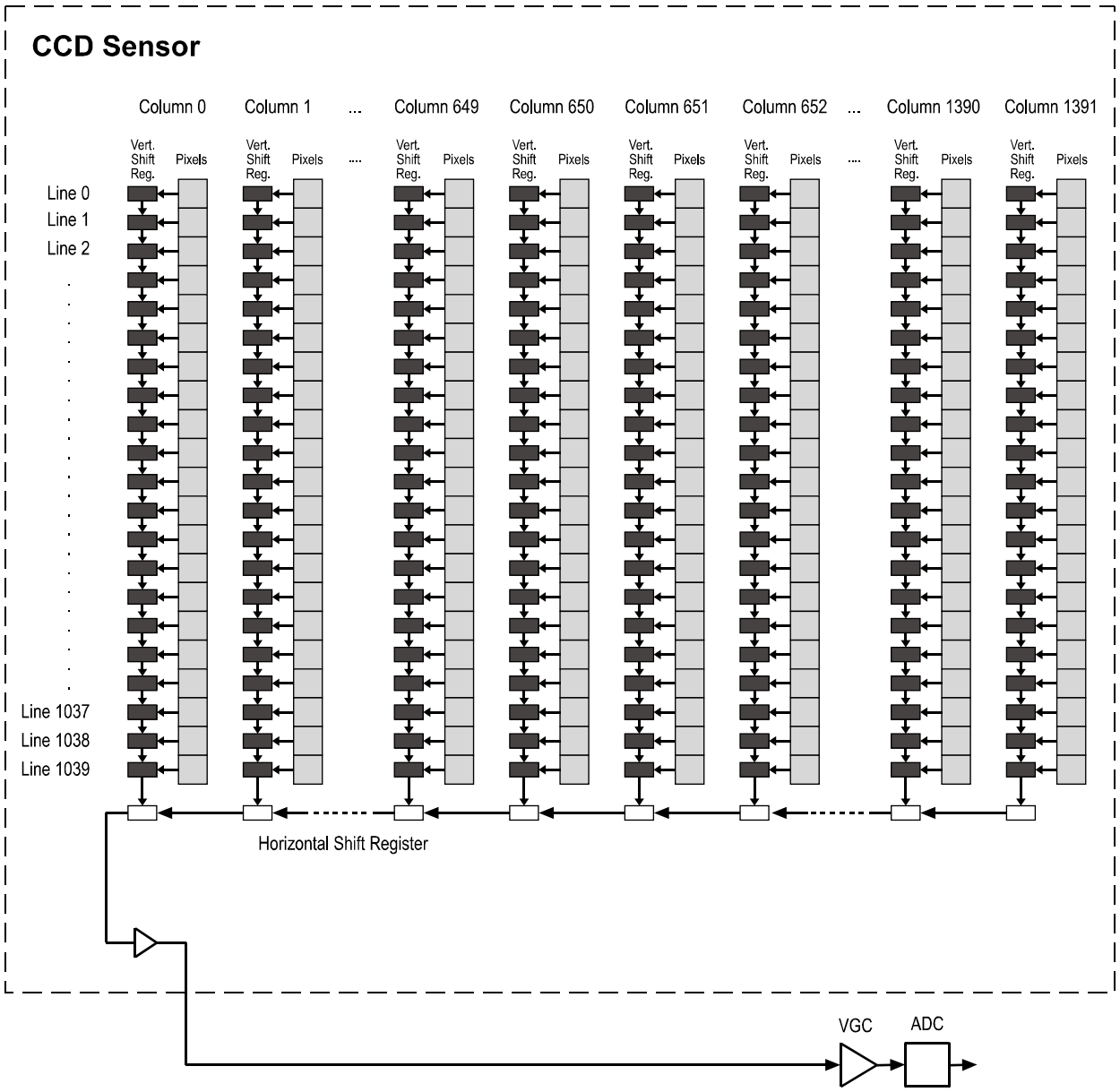

Figure 3-1: **A102f** Sensor Architecture

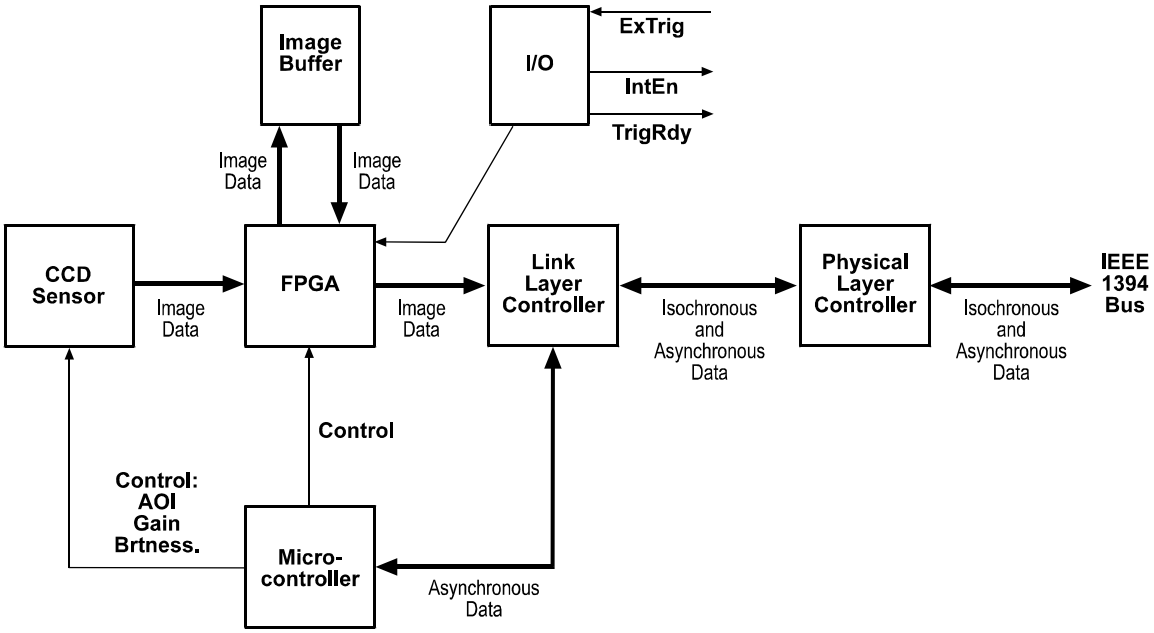

Figure 3-2: Block Diagram

3.2 Exposure Control

3.2.1 Setting the Exposure Time

Exposure time is determined by a combination of two values. The first is the setting in the Value field of the Shutter control register (see page 4-22). The second is the Shutter Time Base. Exposure time is determined by the product of these two values:

Exposure Time = (Shutter Value Setting) x (Shutter Time Base)

The shutter time base is fixed at 20 µs by default. Exposure time is normally adjusted by changing the setting in the Value field of the Shutter control register. The shutter value setting can range from 1 to 4095 (0x001 to 0xFFF). So if the Value field of the Shutter register is set to 100 (0x064), for example, the exposure time will be 100 x 20 µs or 2000 µs.

As mentioned above, the shutter time base is normally fixed at 20 µs and the exposure time is normally adjusted by changing the shutter value setting. However, if you require an exposure time that is shorter or longer than what you can achieve by changing the shutter value alone, the shutter time base can also be changed. The Shutter Time Base smart feature can be used to change the shutter time base. For more information on changing the shutter time base, see Section 6.7.13.

On cameras with a firmware ID number (see Section 1.1) lower than 27, an extra 38 µs was automatically added to the exposure time. For example, if you set the Shutter register to 100 as described above, the actual exposure time would be 2038 µs rather than the expected 2000 µs. On cameras with a firmware ID number of 27 and up, the extra 38 µs is no longer added to the exposure time.

3.2.2 Maximum Exposure Time

The maximum exposure time for a given frame rate is determined by the following formula:

$$\frac{1}{\text{frame rate}} = \text{maximum exposure time}$$

For example, if a camera is operating at 15 fps:

$$\frac{1}{15\ \text{fps}} = 0.0667\ \text{s}$$

So in this case, the maximum exposure time is 66.7 ms.

Exceeding the maximum exposure time for your frame rate will cause the camera to slow down, i.e., it will cause the camera to operate at a lower frame rate.

3.2.3 Controlling Exposure Start with “Shot” Commands via the 1394 Interface

Exposure start can be controlled by sending “shot” commands directly to the camera via the 1394 bus. In this case, a software trigger or an external trigger (ExTrig) signal is not used. When exposure start is controlled with shot commands via the 1394 bus, two modes of operation are available: one-shot and continuous-shot.

One-Shot Operation

In one-shot operation, the camera exposes and transmits a single image. Exposure begins after the One Shot field of the One Shot/Multi Shot control register is set to 1 (see page 4-17). Exposure time is determined by the shutter settings described in Section 3.2.1.

The One Shot field is self cleared after transmission of the image data.

Continuous-Shot Operation

In continuous-shot operation, the camera continuously exposes and transmits images. The exposure of the first image begins after the Continuous Shot field of the ISO En/Continuous Shot control register is set to 1 (see page 4-17). The exposure time for each image is determined by the shutter settings described in Section 3.2.1. The start of exposure on the second and subsequent images is automatically controlled by the camera.

If the camera is operating in video Format 0, the rate at which images will be captured and transmitted is determined by the setting in the Frame Rate field of the Current Video Frame Rate/ Revision control register (see page 4-15).

If the camera is operating in video Format 7, the rate at which images will be captured and transmitted is determined by the setting in the Bytes Per Packet field of the Bytes Per Packet control register (see Section 3.12.2 and page 4-31).

Image exposure and transmission stop after the Continuous Shot field of the ISO En/Continuous Shot control register is set to 0.

These explanations of exposure start are included to give users a basic insight into the interactions of the camera’s registers. Typically, IEEE 1394 cameras are used with a driver which includes an interface that allows the user to parameterize and operate the camera without directly setting registers. The Basler BCAM 1394 Camera Driver, for example, has both a simple Windows® interface and a programmer’s API for parameterizing and operating the camera.

On **A102f** cameras, exposure of a new image can begin while the previous image is being read out. This is commonly referred to as “overlap mode.” Following the recommended method for exposure start in Section 3.2.6 will allow you to overlap exposure with readout and achieve the camera’s maximum frame rate.

3.2.4 Controlling Exposure Start with a Software Trigger

Exposure start can be controlled by sending a software trigger command to the camera via the 1394 bus. The Trigger Mode control register (see page 4-24) is used to enable the ability to start image exposure with a software trigger. The Software Trigger control register (see page 4-19) is used to set the software trigger.

If you are triggering the camera with a software trigger, only the programmable exposure mode is available. In programmable mode, exposure starts when the Trigger field of the Software Trigger control register is set to 1. The length of the exposure is determined by the shutter settings described in Section 3.2.1. The Trigger field will self clear shortly after exposure start. Figure 3-3 illustrates programmable exposure with a software trigger.

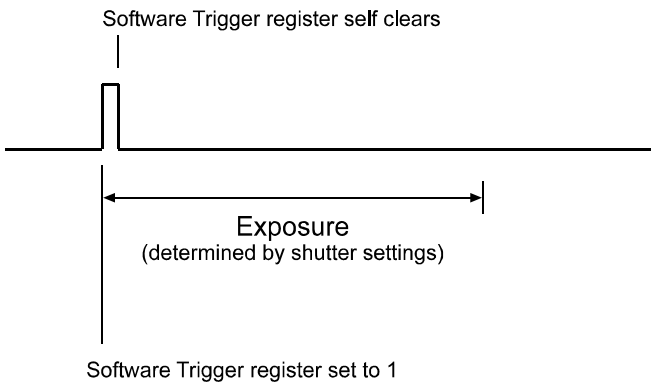

Figure 3-3: Programmable Exposure with a Software Trigger

Enabling the Software Trigger Feature

To enable the software trigger feature:

- Set the On/Off field of the Trigger Mode control register to 1 to enable triggering.
- Set the Trigger Source field of the Trigger Mode control register to 7 to select software triggering.
- Set the Trigger Mode field of the Trigger Mode control register to 0 to select the programmable exposure mode.

Using the Software Trigger Feature

To use the software trigger feature, the camera must be set for continuous-shot operation. If more precise control of exposure start time is desired, you should also monitor the Trigger Ready signal and you must base the timing of the software trigger on the state of the Trigger Ready signal. (See Section 3.3 for more information on the Trigger Ready signal.)

The following descriptions assume that you are using a software trigger to start exposure and that you are monitoring the Trigger Ready signal.

Software Trigger / Continuous-Shot Operation

In Software Trigger/Continuous-shot operation, a “Continuous Shot Command” is used to prepare the camera to capture multiple images. With this method of operation, exposure will begin when the Trigger field of the Software Trigger control register is set to 1. To use this operating method, follow this sequence:

1. Use the shutter settings described in Section 3.2.1 to set your desired exposure time.
2. Set the Continuous Shot field of the ISO En/Continuous Shot control register to 1 (see page 4-17).
3. Check the state of the TrigRdy signal:
   a) If TrigRdy is high, you can set the Trigger field of the Software Trigger register to 1 when desired.
   b) If TrigRdy is low, wait until TrigRdy goes high and then set the Trigger field to 1 when desired.
4. When the Trigger field is set to 1, exposure will begin. (Note that the Trigger field self-clears shortly after exposure begins.)
5. Exposure will continue for the length of time you specified in step 1.
6. At the end of the specified exposure time, readout and transmission of the captured image will take place.
7. Repeat steps 3 and 4 each time you want to begin exposure and capture an image.
8. To disable continuous-shot operation, set the Continuous Shot field in the ISO En/Continuous Shot control register to 0.

The Software Trigger register and the Trigger Source field of the Trigger Mode control register are defined in version 1.31 of the IIDC specification.

Because the software trigger feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the Software Trigger and Trigger Mode registers. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

Why Use the Software Trigger?

At first glance, using the software trigger feature to start image exposure appears to be equivalent to just issuing a one-shot command as described in Section 3.2.3. The difference is in the way the camera reacts to each method. With a one-shot command, there will be some delay between the One Shot field of the One Shot/Multi Shot control register being set to 1 and the actual start of exposure time. This delay is required so that the camera can be properly set up to react to the receipt of the one-shot command. With the software trigger method, there is no delay between the Trigger field being set to 1 and the start of exposure. Exposure begins immediately when the field value is set. So the advantage of the software trigger feature is that it gives you more precise control of exposure start.

On **A102f** cameras, exposure of a new image can begin while the previous image is being read out. This is commonly referred to as “overlap mode.” Following the recommended method for exposure start in Section 3.2.6 will allow you to overlap exposure with readout and achieve the camera’s maximum frame rate.

3.2.5 Controlling Exposure Start with an ExTrig Signal

An external trigger (ExTrig) input signal can be used to control the start of exposure. A rising edge or a falling edge of the signal can be used to trigger exposure start. The Trigger Mode control register (see page 4-24) is used to enable ExTrig exposure start control, to select rising or falling edge triggering, and to assign a physical input port to receive the ExTrig signal.

The ExTrig signal can be periodic or non-periodic. When the camera is operating under control of an ExTrig signal, the period of the ExTrig signal determines the camera's frame rate:

$$\frac{1}{\text{ExTrig period in seconds}} = \text{frame rate}$$

For example, if you are operating a camera with an ExTrig signal period of 110 ms (0.110 sec.):

$$\frac{1}{0.110} = 9.1 \text{ fps}$$

So in this case, the frame rate is 9.1 fps.

The minimum high time for a rising edge trigger (or low time for a falling edge trigger) is 1 µs.

Exposure Modes

If you are triggering the camera with an ExTrig signal, two exposure modes are available, programmable mode and level controlled mode.

Programmable Exposure Mode

When programmable mode is selected, the length of the exposure is determined by the shutter settings described in Section 3.2.1. If the camera is set for rising edge triggering, exposure starts when the ExTrig signal rises. If the camera is set for falling edge triggering, exposure starts when the ExTrig signal falls. Figure 3-4 illustrates programmable exposure with the camera set for rising edge triggering.

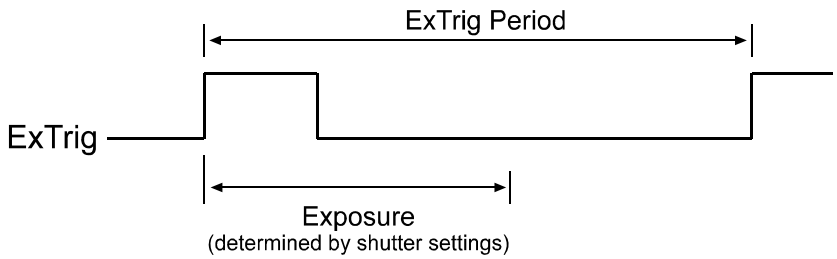

Figure 3-4: Programmable Exposure with Rising Edge Triggering

Level Controlled Exposure Mode

When level controlled mode is selected, the length of the exposure will be determined by the ExTrig signal alone. If the camera is set for rising edge triggering, exposure begins when the ExTrig signal rises and continues until the ExTrig signal falls. If the camera is set for falling edge triggering, exposure begins when the ExTrig signal falls and continues until the ExTrig signal rises. Figure 3-5 illustrates level controlled exposure with the camera set for rising edge triggering.

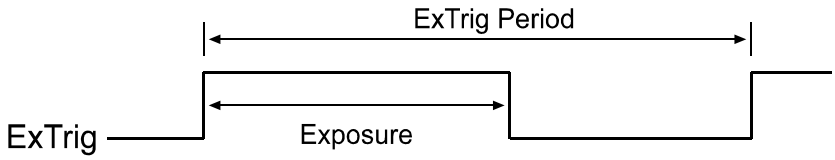

Figure 3-5: Level Controlled Exposure with Rising Edge Triggering

Enabling the External Trigger Feature

To enable the external trigger feature:

- Set the On/Off field of the Trigger Mode control register to 1 to enable triggering.
- Set the Trigger Polarity field of the Trigger Mode control register to 0 to select falling edge triggering or 1 to select rising edge triggering.
- Set the Trigger Mode field of the Trigger Mode control register to 0 to select the programmable exposure mode or 1 to select the level controlled exposure mode.
- Set the Trigger Source field in the Trigger Mode control register to select which one of the four physical input ports on the camera will be used to receive the external trigger signal:
  - Set the Trigger Source field to 0 to select physical input port 0 to receive the ExTrig signal.
  - Set the Trigger Source field to 1 to select physical input port 1 to receive the ExTrig signal.
  - Set the Trigger Source field to 2 to select physical input port 2 to receive the ExTrig signal.
  - Set the Trigger Source field to 3 to select physical input port 3 to receive the ExTrig signal.

The default setting is for physical input port 0 to receive the ExTrig signal. Refer to Sections 2.5.1 and 2.5.2 for a description of the physical and electrical characteristics of the physical input ports.

The Trigger Source field in the Trigger Mode register is defined in version 1.31 of the IIDC specification.

Because the Trigger Source feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the Trigger Source field. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

The ExTrig signal must be used in combination with a one-shot or a continuous-shot command. If more precise control of exposure start time is desired, you must also monitor the Trigger Ready signal and you must base the timing of the ExTrig signal on the state of the Trigger Ready signal. (See Section 3.2.6 for recommended methods for using the signal)

The following descriptions assume that the ExTrig signal is set for rising edge triggering and the programmable exposure mode.

ExTrig / One-Shot Operation

In ExTrig/One-shot operation, a “One-shot” Command is used to prepare the camera to capture a single image. When the ExTrig signal rises, exposure will begin. To use this operating method, follow this sequence:

1. Use the shutter settings described in Section 3.2.1 to set your desired exposure time.
2. Set the One Shot field of the One Shot/Multi Shot control register to 1.
3. Check the state of the TrigRdy signal:
   a) If TrigRdy is high, you can toggle ExTrig when desired.
   b) If TrigRdy is low, wait until TrigRdy goes high and then toggle ExTrig when desired. (See Section 3.3 for more about TrigRdy.)
4. When ExTrig rises, exposure will begin. Exposure will continue for the length of time you specified in step 1.
5. At the end of the specified exposure time, readout and transmission of the captured image will take place.

The One Shot field of the One Shot/Multi Shot control register is self cleared after image transmission.

ExTrig / Continuous-Shot Operation

In ExTrig/Continuous-shot operation, a “Continuous-shot” command is used to prepare the camera to capture multiple images. With this method of operation, exposure will begin on each rising edge of the ExTrig signal. To use this operating method, follow this sequence:

1. Use the shutter settings described in Section 3.2.1 to set your desired exposure time.
2. Set the Continuous Shot field of the ISO En/Continuous Shot control register to 1 (see page 4-17)
3. Check the state of the TrigRdy signal:
   a) If TrigRdy is high, you can toggle ExTrig when desired.
   b) If TrigRdy is low, wait until TrigRdy goes high and then toggle ExTrig when desired. (See Section 3.3 for more about TrigRdy.)
4. When ExTrig rises, exposure will begin. Exposure will continue for the length of time you specified in step 1.
5. At the end of the specified exposure time, readout and transmission of the captured image will take place.
6. Repeat steps 3 and 4 each time you want to begin exposure and capture an image.
7. To disable continuous-shot operation, set the Continuous Shot field in the ISO En/ Continuous Shot control register to 0.

These explanations of exposure start are included to give the user a basic insight into the interactions of the camera's registers. Typically, IEEE 1394 cameras are used with a driver which includes an interface that allows the user to parameterize and operate the camera without directly setting registers. The Basler BCAM 1394 Camera Driver, for example, has both a simple Windows® interface and a programmer's API for parameterizing and operating the camera.

On **A102f** cameras, exposure of a new image can begin while the previous image is being read out. This is commonly referred to as "overlap mode." Following the recommended method for exposure start in Section 3.2.6 will allow you to overlap exposure with readout and achieve the camera's maximum frame rate.

3.2.6 Recommended Method for Controlling Exposure Start

The camera can be programmed to begin exposure on a rising edge or on a falling edge of an ExTrig signal. Also, two modes of exposure control are available: programmable and level controlled (see Section 3.2.5). For this illustration, we are assuming that a rising edge trigger and the programmable exposure mode are used.

If a camera user requires close control of exposure start, there are several general guidelines that must be followed:

- The camera should be placed in continuous shot mode.
- The user must use an external trigger (ExTrig) signal to start exposure.
- The user must monitor the trigger ready (TrigRdy) signal.
- A rising edge of the ExTrig signal must only occur when the TrigRdy signal is high.

Assuming that these general guidelines are followed, the reaction of the camera to a rising external trigger signal will be as shown in Figure 3-6:

- The start of exposure will typically occur between 0 µs and 63 µs after the rise of the ExTrig signal.
- The integrate enabled (IntEn) signal will rise between 5 and 20 µs after the start of exposure.
- The actual length of exposure will be equal to the programmed exposure time.
- The IntEn signal will fall between 30 and 100 µs after the end of exposure.

3.2.7 Frame Buffering

As shown in Figure 3-6, after each image is captured, the camera begins reading out the captured image data from the CCD sensor into a buffer in the camera. When the camera has determined that a sufficient amount of image data has accumulated in the buffer, it will begin transmitting the image data from the camera to the host PC.

This buffering technique avoids the need to exactly synchronize the clock used for sensor readout with the clock used for data transmission over the IEEE 1394 bus. The camera will begin transmitting data when it has determined that it can safely do so without over-running or under-running the buffer. This buffering technique is also an important element in achieving the highest possible frame rate with the best image quality.

The **frame readout time** is the amount of time it takes to read out a captured image from the CMOS sensor into the image buffer.

The **frame transmission time** is the amount of time it takes to transmit the captured image from the buffer in the camera to the host PC via the IEEE 1394 bus.

The **transmission start delay** is the amount of time between the point where the camera begins reading out a captured image into the buffer to the point where it begins transmitting the data for the captured image from the buffer to the host PC.

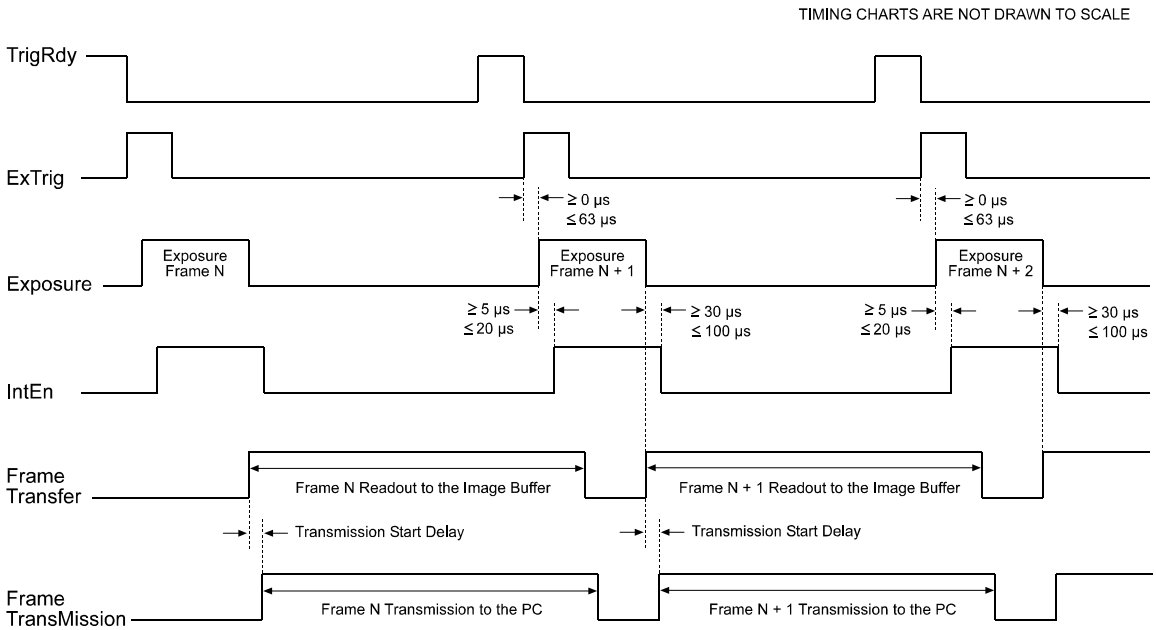

Figure 3-6: Exposure Start Controlled with an ExTrig Signal

You can calculate the frame readout time with this formula:

Frame Readout Time = (AOI Height x 51.2281 µs) + 9941.0 µs

You can calculate the frame transmission time with this formula:

Frame Transmission Time = Packets/frame x 125 µs

To calculate the transmission start delay, use this information:

If the transmission time is greater than the readout time:

Transmission Start Delay = 125 µs.

If the transmission time is less than the readout time:

Transmission Start Delay = (Readout Time - Transmission Time) + 125 µs

3.3 Trigger Ready Signal

The trigger ready signal is not defined in the 1394 Trade Association Digital Camera Specification. Trigger ready is a patented feature of Basler cameras that allows our cameras to have optimized timings.

The maximum frame rate for the camera can be limited by any one of three factors:

- The amount of time it takes to read out a captured image from the CCD sensor to the frame buffer.
- The amount of time it takes to transmit an image from the frame buffer to the PC via the IEEE 1394 bus.
- The exposure time setting.

The camera automatically recalculates the maximum frame rate any time a setting that effects one or more of these factors is changed. For example, the camera will recalculate the maximum frame rate if you change the exposure time, the size of the area of interest, or the packet size.

The camera will use the calculated maximum frame rate to generate a “trigger ready” (TrigRdy) signal. The trigger ready signal indicates the earliest moment that each exposure can begin without exceeding the maximum frame rate for the current conditions. The trigger ready signal will go low when each exposure is started and will go high when it is safe for the next exposure to begin (see Figure 3-6).

By default, the TrigRdy signal is assigned to physical output port 1 on the camera. See Section 2.5.2 for a description of the electrical characteristics of the camera’s physical output ports.

The assignment of the TrigRdy signal to a physical output port can be changed. See Section 6.7.11 for more information on changing the assignment of camera output signals to physical output ports.

If you signal the camera to start an exposure when trigger ready is low, the camera will delay the start of exposure until the next rise of the trigger ready signal. This prevents you from running the camera faster than the maximum rate and avoids dropping frames.

If the camera is in continuous shot mode and external triggering is disabled, the trigger ready output signal will not be present.

3.4 Integrate Enabled Signal

The Integrate Enabled (IntEn) signal goes high when exposure begins and goes low when exposure ends. This signal can be used as a flash trigger and is also useful when you are operating a system where either the camera or the object being imaged is movable. For example, assume that the camera is mounted on an arm mechanism and that the mechanism can move the camera to view different portions of a product assembly. Typically, you do not want the camera to move during exposure. In this case, you can monitor the IntEn signal to know when exposure is taking place and thus know when to avoid moving the camera.

By default, the IntEn signal is assigned to physical output port 0 on the camera. See Section 2.5.2 for a description of the electrical characteristics of the camera's physical output ports.

The assignment of the IntEn signal to a physical output port can be changed. See Section 6.7.11 for more information on changing the assignment of camera output signals to physical output ports.

When you use the integrate enabled signal, be aware that there is a delay in the rise and the fall of the signal in relation to the start and the end of exposure. See Figure 3-6 for details.

3.5 Gain and Brightness

The major components in the **A102f** electronics include: a CCD sensor, one VGC (Variable Gain Control), and one ADC (Analog to Digital Converter). The pixels in the CCD sensor output voltage signals when they are exposed to light. These voltages are amplified by the VGC and transferred to the ADC which converts the voltages to digital output signals.

Two parameters, gain and offset are associated with the VGC. As shown in Figures 3-7 and 3-8, increasing or decreasing the gain increases or decreases the amplitude of the signal that is input to the ADC. Increasing or decreasing the offset moves the signal up or down the measurement scale but does not change the signal amplitude.

For most applications, black should have a gray value of 1 and white should have a gray value of 255 (in modes that output 8 bits per pixel) or 4095 (in modes that output 12 effective bits per pixel). Attempt to achieve this by varying exposure and illumination rather than changing the camera's gain. The default gain is the optimal operating point (minimum noise) and should be used if possible.

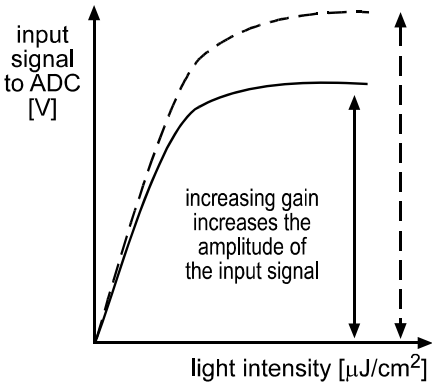

Figure 3-7: Gain

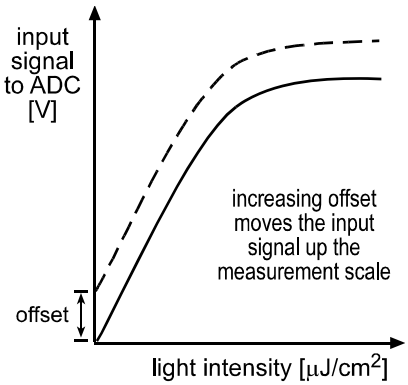

Figure 3-8: Offset

Because increasing gain increases both signal and noise, the signal to noise ratio does not change significantly when gain is increased.

3.5.1 Setting Gain

When the gain is set to default, the sensor's linear output range directly matches the input voltage range of the ADC. Thus, with the default gain of 0 dB, a gray value of 1 is produced when the pixels are exposed to no light and a gray value of 255 (in modes that output 8 bits per pixel) or 4095 (in modes that output 12 effective bits per pixel) is produced when the pixels are exposed to bright light.

0 dB of gain is achieved when gain is programmed to a decimal value of 192. Increasing the gain setting to more than 192 maps a smaller portion of the sensor's linear output range to the ADC's input.

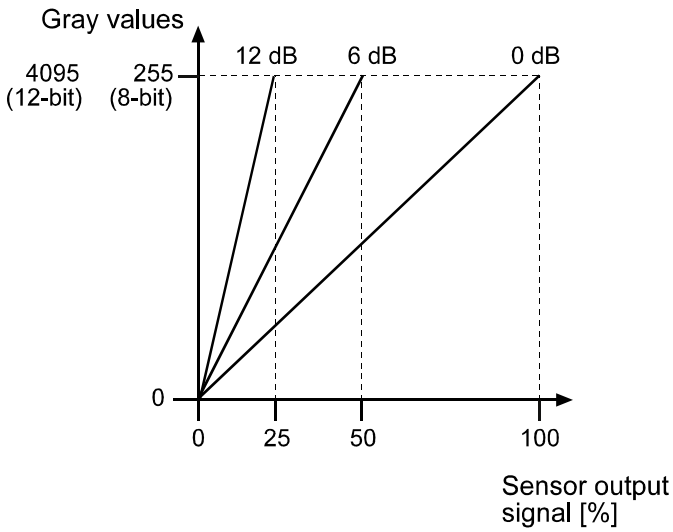

Figure 3-9: Gain Settings in dB

Increasing the gain is useful when at your brightest exposure, a gray value lower than 255 (in modes that output 8 bits per pixel) or 4095 (in modes that output 12 effective bits per pixel) is reached. For example, if you found that at your brightest exposure your gray values were no higher than 127 (8-bit mode), you could increase the gain to 6 dB (amplification factor of 2) and thus reach gray values of 254 (see Figure 3-9).

Gain is adjustable and can be programmed on a decimal scale that ranges from 192 to 1023 (0x0C0 to 0x3FF). The camera's gain is determined by the setting in the Value field of the Gain control register (see page 4-23).

If you know the decimal number (DN) setting for the gain on your camera, the equivalent decibel value can be calculated using one of the following equations:

When DN setting = 192 to 511

$$dB = 20 \times \log_{10}\left(\frac{658 + DN}{658 - DN}\right) - 5.221$$

When DN setting = 512 to 1023

$$dB = 0.0354 \times DN - 5.221$$

When the camera is set for Mono 16 output, only settings from 192 to 511 are valid. Settings above 511 should not be used with the camera set for Mono 16 output. In all other output modes, the entire 192 to 1023 range of gain settings is valid.

In normal operation, a gain setting lower than 192 should not be used. When the gain setting is lower than 192, the sensor output signal that is mapped to the input of the ADC will not be linear.

The gain settings result in the following amplifications:

Decimal Number (DN)	Hexadecimal	dB	Factor
192	0x0C0	0	X1
374	0x176	6	X2
499	0x1F3	12	X4
656	0x290	18	X8
825	0x339	24	X16
1023	0x3FF	31	X35.5

Table 3-1: Examples of Gain Settings in dB

3.5.2 Setting Brightness

The camera's brightness is determined by the setting in the Value field of the Brightness control register (see page 4-20). The brightness setting can be programmed on a decimal scale that ranges from 0 to 255, (0x000 to 0x0FF).

If the camera is operating in any output mode other than Mono 16, a brightness setting of around 8 (decimal) will result in an offset of 0 in the digital values output for the pixels. (Due to tolerances in the electronic components in your camera, you may find that the default brightness is set to a slightly different setting.) An increase of 16 (decimal) in the brightness setting will result in a positive offset of 1 in the digital values output for the pixels. For example, a brightness setting of around 24 (8 + 16, decimal) would be required to reach a positive offset of 1. A brightness setting of around 40 (8 + 16 + 16, decimal) would be required to reach a positive offset of 2, and so on.

If the camera is set for Mono 16 output, a brightness setting of around 0 (decimal) will result in an offset of 0 in the digital values output for the pixels. An increase of 1 (decimal) in the brightness setting will result in a positive offset of 1 in the digital values output for the pixels.

3.6 Area of Interest (AOI)

The area of interest (AOI) feature allows you to specify a portion of the CCD array and during operation, only the pixel information from the specified portion of the array is transmitted out of the camera.

The area of interest is referenced to the top left corner of the CCD array. The top left corner is designated as column 0 and row 0 as shown in Figure 3-10.

The location and size of the area of interest is defined by declaring a left-most column, a width, a top row and a height. For example, suppose that you specify the left column as 10, the width as 16, the top row as 4 and the height as 10. The area of the array that is bounded by these settings is shown in Figure 3-10.

The camera will only transmit pixel data from within the area defined by your settings. Information from the pixels outside of the area of interest is discarded.

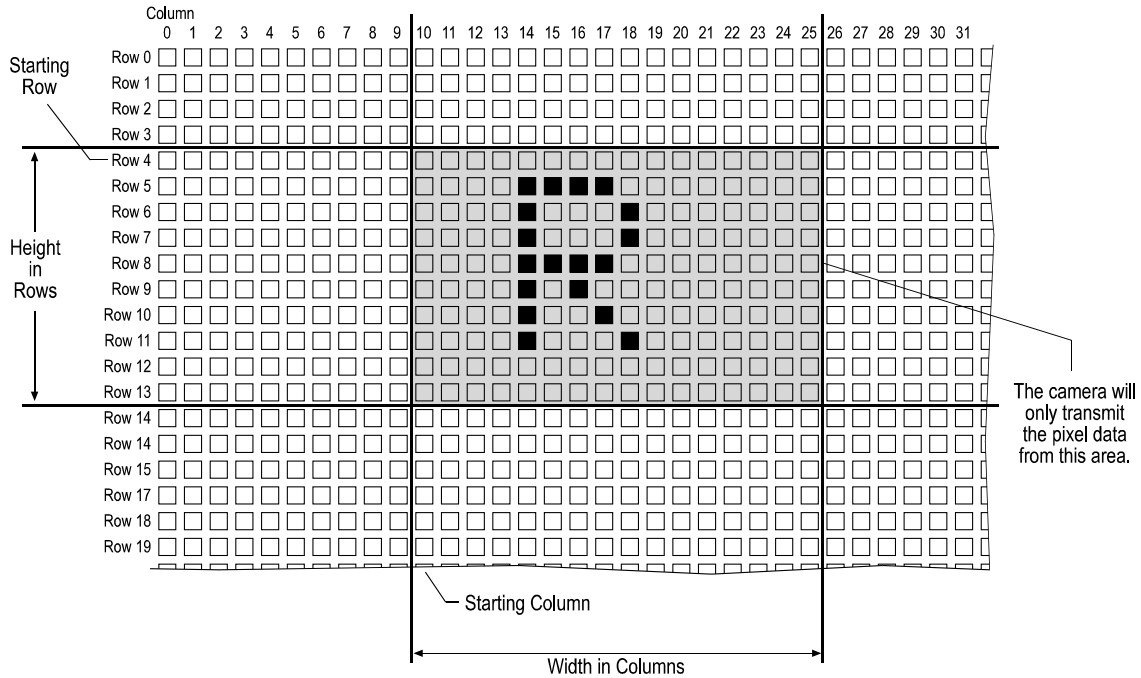

Figure 3-10: Area of Interest

The AOI feature is enabled by setting the camera to operate in Format 7, Mode 0. This is accomplished by setting the Format field of the Current Video Format control register (see page 4-16) to 7 and the Mode field of the Current Video Mode control register to 0.

The location of the area of interest is defined by setting a value for the Left field and a value for the Top field of the Image Position control register for Format 7, Mode 0 (see page 4-28). The size of the area of interest is defined by setting a value for the Width field and a value for the Height field of the Image Size control register for Format 7, Mode 0.

To use the entire CCD array in the **A102f** monochrome cameras, set the value for Left to 0, the value for Top to 0, the value for Width to 1392 and the value for Height to 1040.

To use the entire CCD array in the **A102fc** color cameras, set the value for Left to 0, the value for Top to 0, the value for Width to 1388 and the value for Height to 1038.

The sum of the setting for *Left* plus the setting for *Width* must not exceed 1392 for **A102f** monochrome cameras or 1388 for **A102fc** color cameras.

The sum of the setting for *Top* plus the setting for *Height* must not exceed 1040 for **A102f** monochrome cameras or 1038 for **A102fc** color cameras.

When you are setting the AOI on an **A102fc** color camera:

- The setting for *Width* must be divisible by 2.
- The setting for *Height* must be divisible by 2.
- The setting for *Left* must be zero or be divisible by 2.
- The setting for *Top* must be zero or be divisible by 2.

3.6.1 Changing AOI Parameters “On-the-Fly”

Making AOI parameter changes “on-the-fly” means making the parameter changes while the camera is capturing images continuously. On-the-fly changes are only allowed for the parameters that determine the position of the AOI, i.e., the parameters for top and left. Changes to the AOI size are not allowed on-the-fly.

The camera’s response to an on-the-fly change in the AOI position will vary depending on the way that you are operating the camera:

- If the exposure time is ≥ 100 µs, the changes will take effect on the next trigger after the changes are received by the camera.
- If the exposure time is < 100 µs and the camera is running in non-overlapped mode[1], the changes will take effect on the next trigger after the changes are received by the camera.
- If the exposure time is < 100 µs and the camera is running in overlapped mode[2], when the changes are received by the camera, the camera will delay the triggering of the next image until transmission of the current image is complete. When transmission of the current image is complete, the camera will change the AOI position, will trigger the next image, and will resume running in overlapped mode.

[1] The term “non-overlapped” mode means that image capture is triggered in the following manner: the camera captures (exposes) an image and completely transmits that image out of the camera before the next image capture is triggered. In other words, exposure and transmission of image N are both completed before exposure of image N+1 begins.

[2] The term “overlapped” mode means that image capture is triggered in the following manner: the camera captures (exposes) an image and while this image is being transmitted out of the camera, capture of the next image is triggered. In other words, capture of image N+1 begins while transmission of image N is still in progress.

3.6.2 Changes to the Frame Rate with AOI

In general, the maximum frame rate for the camera increases as the size of the AOI decreases. However, the maximum frame rate can also be limited by any one of three factors:

- The amount of time it takes to read out a captured image from the image sensor to the frame buffer.
- The amount of time it takes to transmit an image from the frame buffer to the PC via the IEEE 1394 bus.
- The exposure time setting.

To determine the maximum frame rate for a given AOI, use your AOI and exposure time settings to calculate a result in each of the three formulas below. These formulas take your AOI size into account plus the three factors that can limit the frame rate. The formula that returns the lowest value will determine the maximum frame rate for the given AOI.

Formula 1 calculates the maximum frame rate based on the sensor readout time:

$$\text{Max Frames/s} = \frac{1}{(\text{AOI Height} \times 51.2281\ \mu s) + 9941.0\ \mu s}$$

Formula 2 calculates the maximum frame rate based on the frame transmission time:

$$\text{Max. Frames/s} = \frac{1}{\text{Packets/frame} \times 125\ \mu s}$$

Formula 3 calculates the maximum frame rate based on the exposure time:

$$\text{Max. Frames/s} = \frac{1}{\text{Exposure Time in } \mu s + 181.1\ \mu s}$$

Example

Assume that your camera is set for Format 7, Mode 0, that your AOI is set for 100 columns wide and 110 rows high and that your exposure time is set for 12000 µs. Also assume that after making all camera settings, you check the Packets Per Frame Inquiry register in the control and status registers for Format 7, Mode 0. You find that the packets per frame with the current settings is 3.

The number of packets per frame depends on the setting of the Format 7, Mode 0 Bytes Per Packet control register. In this example, we assume that the bytes per packet is set to the maximum. See Sections 3.12.2 and 3.13.2 for more information.

Formula 1:

$$\text{Max Frames/s} = \frac{1}{(110 \times 51.2281\ \mu s) + 9941.0\ \mu s}$$

Max. Frames/s = 64.2

Formula 2:

$$\text{Max. Frames/s} = \frac{1}{3 \times 125\ \mu s}$$

Max. Frames/s = 2666.7

Formula 3:

$$\text{Max. Frames/s} = \frac{1}{12000\ \mu s + 181.1\ \mu s}$$

Max. Frames/s = 82.1

Formula one returns the lowest value. So in this case, the limiting parameter is the frame readout time and the maximum frame rate would be 64.2 frames per second.

3.7 Low Smear

In applications where a CCD sensor is under constant illumination, high-contrast images may show an unwanted effect that converts dark pixels into brighter ones. This effect is commonly called “smearing“.

With the help of the Low Smear feature on the **A102f**, smearing is reduced in the upper part of the image. The effect of the Low Smear feature is illustrated in Figure 3-11.

The left image was captured without the low smear feature. There is smearing both in the upper and lower part of the image.

The right image was captured with low smear active. There is no smearing in the upper part of the image.

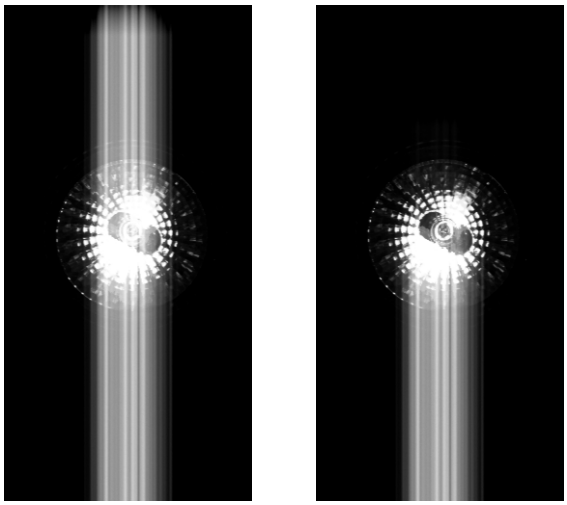

Figure 3-11: Full Smear (left), Low Smear (right)

Smearing is caused by two things:

- An unwanted post-exposure of the pixels when they are being moved out through the vertical shift registers. Only those pixels located above the area of exposure on the CCD array which must pass the light source during shift-out are subject to post-exposure. For this reason, post-exposure only produces smearing in the lower part of the image. (Remember that the lens causes the image on the sensor to be inverted, so the lower part of the image is at the top of the sensor.)
- An unwanted existing accumulation of charges in those shift registers which have passed points of constant illumination during the previous frame readout and have thus been exposed before they receive the next pixels. These unwanted charges add to the next pixels when these pixels are shifted from the sensor cells into the vertical shift registers. This causes smearing in the upper part of the image.

The amount of unwanted charges accumulated in the shift registers grows with the amount of exposure. For that reason, smearing does not appear under short-term illumination such as flash light. It only appears under constant illumination.

The Low Smear feature cannot be activated or deactivated. It is active all of the time. To use this feature to its best advantage, the frame rate must not exceed a maximum setting. The setting can be calculated using the equation below.

$$\text{Frames/s} \leq \frac{1}{(\text{AOIH} \times 51.2281\ \mu\text{s}) + 16879.0\ \mu\text{s}}$$

where: AOIH = number of lines in the AOI

For example, with a 1392 (H) x 600 (V) area of interest, the calculation looks like this:

Frames/s ≤ (600 x 51.2281 µs) + 16879.0 µs

Frames/s ≤ 21.0

If the camera's actual frame rate is higher than the maximum recommended frame rate, the smearing will return. When you exceed the maximum recommended frame rate by a small amount, the upper part of the image will show partial smearing (Figure 3-12). As the frame rate is increased, the smearing will become worse.

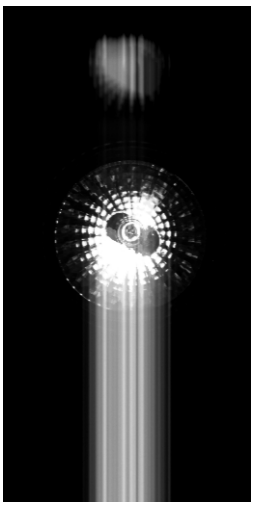

Figure 3-12: Partial Smear

3.8 Color Creation in the A102fc

The CCD sensor used in the **A102fc** is equipped with an additive color separation filter known as a Bayer filter. With the Bayer filter, each individual pixel is covered by a micro-lens which allows light of only one color to strike the pixel. The pattern of the Bayer filter used in the **A102fc** is shown in Figure 3-13. As the figure illustrates, within each block of four pixels, one pixel sees only red light, one sees only blue light, and two pixels see only green light. (This combination mimics the human eye's sensitivity to color.)

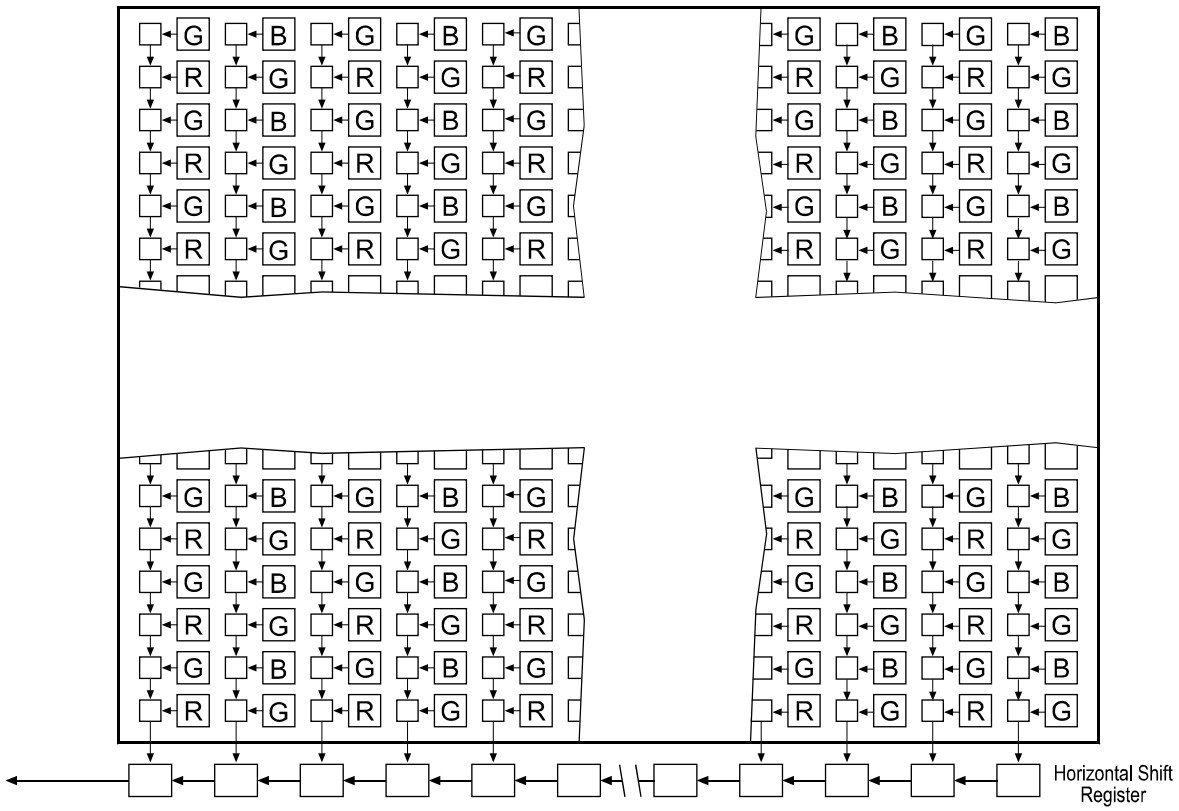

Figure 3-13: Bayer Filter Pattern on the **A102fc**

When an **A102fc** is operating in a YUV color output mode, each pixel goes through a two step conversion process as it exits the sensor and passes through the camera's electronics.

In the first step of the process an interpolation algorithm is performed to get full RGB data for the pixel. (Because each individual pixel gathers information for only one color, an interpolation must be made from the surrounding pixels to get full RGB data for an individual pixel.)

The second step of the process is to convert the RGB information to YUV. The conversion algorithm uses the following formulas:

$Y = 0.30\,R + 0.59\,G + 0.11\,B$

$U = -0.17\,R - 0.33\,G + 0.50\,B$

$V = 0.50\,R - 0.41\,G - 0.09\,B$

Once the conversion to YUV is complete, pixels are transmitted from the camera in the YUV (4:2:2) format as defined in Sections 5.3 and 5.4.

The values for U and for V normally range from -128 to +127. Because the 1394 Digital Camera specification requires that U values and V values be transmitted with unsigned integers, 128 is added to each U value and to each V value before the values are transmitted from the camera. This process allows the values to be transmitted on a scale that ranges from 0 to 255 (see Section 5.4.2).

When an **A102fc** is operating in a YUV (4:2:2) mode, the average number of bits per pixel is 16. This means that the camera will require twice the bandwidth of a camera operating in an 8 bit monochrome mode.

The **A102fc** can operate in YUV (4:2:2) color mode as well as several monochrome 8 bit modes (see Section 3.13).

3.8.1 White Balance

White balance capability has been implemented on the **A102fc**. With white balancing, correction factors are applied to the interpolated RGB values for each pixel. The correction factors can be used to adjust the color balance of the images transmitted from the camera.

The white balancing scheme outlined in the IIDC specification dictates that blue and red are adjustable and that green is not. On **A102fc** cameras, green has a fixed value of 96 (0x60) which corresponds to a correction factor of 1.5. You can effectively raise the relative amount of green by lowering the correction factor for blue and red below 1.5. You can effectively lower the relative amount of green by raising the correction factor for blue and red above 1.5.

The Blue Value field of the White Balance control register (see page 4-21) can be used to change the blue correction factor. The usable range of settings for this field is from 64 (0x40) to 255 (0xFF). If the field is set to 96 (0x60), blue will have the same 1.5 correction factor as green. If the field is set to a lower value, blue will have a lower correction factor and the image will be less blue. If the field is set to a higher value, blue will have a higher correction factor and the image will be more blue. The default setting for the Blue Value is 151 (0x97).

To determine the correction factor for blue, use this formula:

$$\text{Blue Correction Factor} = \frac{\text{Blue Value Setting}}{64}$$

The Red Value field of the White Balance control register can be used to change the red correction factor. The usable range of settings for the this field is from 64 (0x40) to 255 (0xFF). If the field is set to 96 (0x60), red will have the same 1.5 correction factor as green. If the field is set to a lower value, red will have a lower correction factor and the image will be less red. If the field is set to a higher value, red will have a higher correction factor and the image will be more red. The default setting for the Red Value is 122 (0x7A).

To determine the correction factor for red, use this formula:

$$\text{Red Correction Factor} = \frac{\text{Red Value Setting}}{64}$$

The actual range of valid settings for the Blue Value is from 16 (0x10) to 255 (0xFF), however, only the settings from 64 (0x40) to 255 (0xFF) are useful. If you set the Blue Value lower than 64 (0x40), the camera will continue to operate, but you will see unacceptable changes in the color balance.

The actual range of valid settings for the Red Value is from 16 (0x10) to 255 (0xFF), however, only the settings from 64 (0x40) to 255 (0xFF) are useful. If you set the Red Value lower than 64 (0x40), the camera will continue to operate, but you will see unacceptable changes in the color balance.

3.8.2 Color Filter ID

The Color Filter ID register for Format 7 (see page 4-32) has been implemented on **A102f** cameras. This Color Filter ID register can be used to determine the alignment of the camera's color filter to the current Area of Interest (AOI). To use this feature, make all desired changes to the camera's parameter settings and then read the value in the Filter ID field of the Color Filter ID register. The field will indicate an ID of 0, 1, 2, or 3 as appropriate.

As shown in Table 3-2, each ID identifies the color of the first two pixels in the first row of the current AOI and the color of the first two pixels in the second row of the AOI. Due to the repetitive nature of the Bayer RGB primary color filter (see page 3-25) used in the **A102fc**, this information is all you need to determine the order of the pixel colors with your current settings.

	ID 0	ID 1	ID 2	ID 3
First pixel in the first row	R	G	G	B
Second pixel in the first row	G	B	R	G
First pixel in the second row	G	R	B	G
Second pixel in the second row	B	G	G	R

Table 3-2: Color Filter IDs

The Color Filter ID register for Format 7 is defined in version 1.31 of the IIDC specification.

Because the Color Filter ID feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the Filter ID field. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

3.8.3 Integrated IR Cut Filter on C-Mount Equipped Cameras

A102fc color cameras are equipped with an IR cut filter as standard equipment. The filter is mounted in the lens adapter. Cameras without an IR cut filter are available on request.

Caution!

The location of the filter limits the thread length of the lens that can be used on the camera. The thread length on your lens must be less than 7.5 mm. If a lens with a longer thread length is used, the camera will be damaged and will no longer operate. See Section 7.3 for more details.

3.9 Selectable 8 or 12 Bit Pixel Depth

When an **A102f** camera is operating in Format 7, it can be set to output pixel data at either 8 bit or 12 bit depth.

3.9.1 A102f Monochrome Cameras

Set the value in the Format field of the Current Video Format register (see page 4-16) and the value in the Mode Field of the Current Video Mode register (see page 4-15) so that the camera will operate in Format 7, Mode 0.

For 8 Bit Depth

Set the value in the Coding ID field of the Color Coding ID register for Format 7, Mode 0 to Mono 8 (see Section 3.12.2 and page 4-27). With this ID set, the camera outputs 8 bits per pixel.

For 12 Bit Depth

Set the value in the Coding ID field of the Color Coding ID register for Format 7, Mode 0 to Mono 16. With this ID set, the camera outputs 16 bits per pixel but only 12 bits are effective. The effective pixel data fills from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little endian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address.

3.9.2 A102fc Color Cameras

Set the value in the Format field of the Current Video Format register (see page 4-16) and the value in the Mode Field of the Current Video Mode register (see page 4-15) so that the camera will operate in Format 7, Mode 0.

For 8 bit depth

Set the value in the Coding ID field of the Color Coding ID register for Format 7, Mode 0 to either Mono 8 or Raw 8 (see Section 3.13.2 and page 4-27). With either of these IDs set, the camera outputs 8 bits per pixel.

When the Mono 8 color coding ID is set, the camera outputs 8 bits per pixel and outputs only the Y component (brightness) of the YUV format.

When the Raw 8 color coding ID is set, the camera outputs 8 bits per pixel and outputs the raw data for each pixel. (The pixel data is **not** processed to account for the color filter.)

For 12 bit depth

Set the value Coding ID field of the Color Coding ID register for Format 7, Mode 0 to Raw 16. When the Raw 16 color coding ID is set, the camera outputs 16 bits per pixel and outputs the raw data for each pixel. (The pixel data is **not** processed to account for the color filter.) Although the camera outputs 16 bits per pixel in this mode, only 12 bits are effective. The effective pixel data fills from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little endian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address.

When a camera is operating in a mode that outputs 16 bits per pixel, the maximum frame rate at full resolution is 11.3 fps.

3.10 Strobe Control Output Signals

A102f cameras include a feature designed to help you control strobe lighting. The feature allows a user to enable and parameterize up to four strobe control output signals. The signals are designated as Strobe 0, Strobe 1, Strobe 2, and Strobe 3. The Strobe Signal Function control registers (see page 4-42) are used to enable and parameterize the strobe output signals.

The text below describes using the Strobe Signal Function registers for Strobe 0 to enable and parameterize Strobe 0. Strobe 1, Strobe 2 and Strobe 3 are enabled and parameterized in similar fashion by using the respective registers for each strobe.

Enabling the Strobe 0 Control Feature

To enable the Strobe 0 signal:

- Set the value in the On/Off field of the Strobe 0 Control register to 1.
- Set the value in the Signal Polarity field to 0 for a low active signal or 1 for a high active signal as desired.

Setting the Delay for Strobe 0

The strobe delay is determined by a combination of two values. The first is the setting in the Delay Value field of the Strobe 0 Control register (see page 4-22). The second is the Strobe Delay Time Base. The Strobe 0 delay will be determined by the product of these two values:

Strobe 0 Delay = (Strobe 0 Delay Value Setting) x (Strobe Delay Time Base)

The strobe delay time base is fixed at 1/1024 ms by default. Strobe 0 delay time is normally adjusted by changing the setting in the Delay Value field of the Strobe 0 Control register. The delay value setting can range from 0 to 4095 (0x000 to 0xFFF). So if the setting in the Delay Value field of the Strobe 0 Control register is set to 100 (0x064), for example, the Strobe 0 delay will be 100/1024 ms (or approximately 97.7 µs).

The strobe delay will determine the time between the start of image exposure and when the strobe signal changes state as shown in Figure 3-14.

As mentioned above, the strobe delay time base is normally fixed at 1/1024 ms and the Strobe 0 delay is normally adjusted by changing the delay value setting only. However, if you require a delay that is longer than what you can achieve by changing the strobe delay value alone, the strobe delay time base can also be changed. The Strobe Time Base smart feature can be used to change the strobe delay time base. For more information on changing the strobe delay time base, see Section 6.7.14.

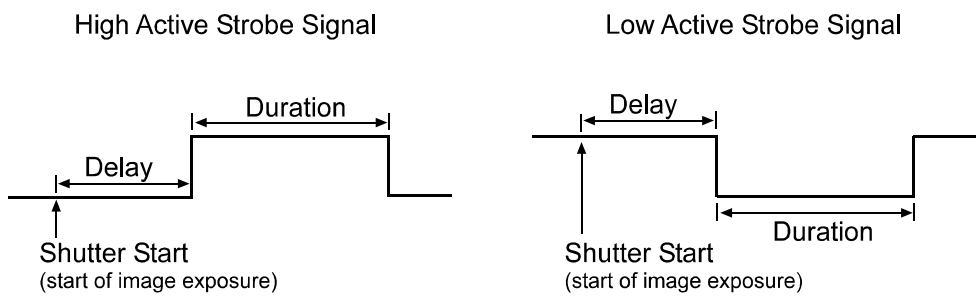

Figure 3-14: Strobe Signal

Setting the Duration for Strobe 0

The strobe duration is determined by a combination of two values. The first is the setting in the Duration Value field of the Strobe 0 Control register (see page 4-22). The second is the Strobe Duration Time Base. Strobe 0 duration will be determined by the product of these two values:

Strobe 0 Duration = (Strobe 0 Duration Value Setting) x (Strobe Duration Time Base)

The strobe duration time base is fixed at 1/1024 ms by default. Strobe 0 duration is normally adjusted by changing the setting in the Duration Value field of the Strobe 0 Control register. The duration value setting can range from 0 to 4095 (0x000 to 0xFFF). So if the setting in the Duration Value field of the Strobe 0 Control register is set to 250 (0x0FA), for example, the Strobe 0 duration will be 250/1024 ms (or approximately 244.1 µs).

The strobe duration will determine the duration of the strobe signal as shown in Figure 3-14.

As mentioned above, the strobe duration time base is normally fixed at 1/1024 ms and the Strobe 0 duration is normally adjusted by changing the duration value setting only. However, if you require a duration that is longer than what you can achieve by changing the strobe duration value alone, the strobe duration time base can also be changed. The Strobe Time Base smart feature can be used to change the strobe duration time base. For more information on changing the strobe delay time base, see Section 6.7.14.

Assigning the Strobe 0 Signal to a Port

Once the Strobe 0 output signal has been enabled and parameterized, **it must be assigned to a physical output port on the camera**. The Strobe 0 signal can only be assigned to physical output port 0. Strobe output signals are assigned to physical ports by using the Output Port Configuration smart feature. See Section 6.7.11 for information on assigning strobe output signals to physical output ports.

If you enable the Strobe 1, Strobe 2 and Strobe 3 output signals, you must also use the Output Port Configuration smart feature to assign these signals to physical output ports on the camera. The Strobe 1 signal can only be assigned to physical output port 1. The Strobe 2 signal can only be assigned to physical output port 2. The Strobe 3 signal can only be assigned to physical output port 3.

If you start an image exposure and the strobe signal for the previously captured image is still running, the running strobe signal ends immediately and the next delay and duration begin.

The Strobe Control Output Signal registers are defined in version 1.31 of the IIDC specification.

Because the strobe control output signal feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the strobe control output signal registers. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

3.11 Parallel Input/Output Control

A parallel I/O control feature is available on **A102f** cameras. The feature allows a user to set the state of the four physical output ports on the camera and to read the state of the four physical input ports.

To set state of the four physical output ports, write values to the fields in the PIO Output register (see page 4-41):

- The value in the Port 0 Out field sets the state of physical output port 0.
- The value in the Port 1 Out field sets the state of physical output port 1.
- The value in the Port 2 Out field sets the state of physical output port 2.
- The value in the Port 3 Out field sets the state of physical output port 3.

Writing to the PIO Output register will only set the state of physical output ports that are configured as “User set.” For any output ports not configured as user set, the bit settings in this register will be ignored. See Section 6.7.11 for information on configuring physical output ports.

To determine the current state of the four physical input ports, read the contents of the PIO Input register (see page 4-41):

- The value in the Port 0 In field indicates the current state of physical input port 0.
- The value in the Port 1 In field indicates the current state of physical input port 1.
- The value in the Port 2 In field indicates the current state of physical input port 2.
- The value in the Port 3 In field indicates the current state of physical input port 3.

The PIO Control registers are defined in version 1.31 of the IIDC specification.

Because the PIO control feature is so new, the Basler BCAM 1394 Driver does not yet include a method call to access this feature. As a work-around, you can use the techniques described in the tutorial for the Basler Smart Features Framework Software to directly read from or write to the PIO registers. The Smart Features Framework Software is available on the Basler web site. To download the software go to:

http://www.baslerweb.com/popups/popup_en_1825.php

3.12 Available Video Formats, Modes and Frame Rates on Monochrome Cameras

3.12.1 Standard Formats, Modes and Frame Rates

The following standard video formats, modes and frame rates are available on all **A102f** monochrome cameras:

Format 2, Mode 2, FrameRate 3 (1280 x 960, Y Mono, 8 bits/pixel, 15 fps)

Format 2, Mode 6, FrameRate 2 (1280 x 960, Y Mono, 16 bits/pixel, 7.5 fps)

When the camera is operating in Format 2, Mode 6, it outputs 16 bits per pixel but only 12 bits are effective. The effective pixel data fills from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little endian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address.

3.12.2 Customizable Formats and Modes

Format 7, Mode 0 is available on **A102f** monochrome cameras.

Format 7, Mode 0

Format 7, Mode 0 is used to enable and set up the area of interest (AOI) feature described in Section 3.6. Format 7, Mode 0 is parameterized by using the Format 7, Mode 0 control and status registers (see page 4-27).

When the camera is operating in Format 7, Mode 0, the frame rate can be adjusted by setting the number of bytes transmitted in each packet. The number of bytes per packet is set by the Bytes Per Packet field of the Bytes Per Packet register.

The value that appears in the Max Bytes Per Packet field of the Packet Para Inquiry register will show the maximum allowed bytes per packet setting given the current AOI settings. When the bytes per packet is set to the maximum, the camera will transmit frames at its maximum specified rate. By default, the AOI is set to use the full sensor area and the bytes per packet is set to 4096.

If you set the bytes per packet to a value lower than the maximum, the camera will transmit frames at a lower rate. The rate is calculated by the formula:

$$\text{Frames/s} = \frac{1}{\text{Packets per Frame} \times 125\ \mu\text{s}}$$

Keep in mind that when you lower the bytes per packet setting, the number of bytes needed to transmit a frame (the packets per frame) will increase. Due to limitations in the DCAM structure, a maximum of 4095 packets per frame is allowed. If you set the bytes per packet too low, the number of packets per frame will exceed the 4095 packet limit and the camera will not transmit frames properly.

When the camera is operating in Format 7, the Current Video Frame Rate control register is not used and has no effect on camera operation.

Color Codings

In Format 7, Mode 0, the Mono 8 and Mono 16 color codings are available.

When the **Mono 8** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs 8 bits per pixel.

When the **Mono 16** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs 16 bits per pixel but only 12 bits are effective. The effective pixel data fills from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little endian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address.

When the camera is set for the Mono 16 color coding, the maximum frame rate at full resolution is 11.3 frames/s.

Color code definitions can very from camera model to camera model. This is especially true for older models of Basler cameras.

3.13 Available Video Formats, Modes and Frame Rates on Color Cameras

3.13.1 Standard Formats, Modes and Frame Rates

The following standard video formats, modes and frame rates are available on **A102fc** color cameras:

Format 2, Mode 0, FrameRate 2 (1280 x 960, YUV 4:2:2, 16 bits/pixel ave, 7.5 fps)

Format 2, Mode 2, FrameRate 3 (1280 x 960, Y Mono, 8 bits/pixel, 15 fps)

When the **A102**fc is operating in Format 2, Mode 2, it outputs the **raw data** for each pixel, not the Y component as indicated in the DCAM specification. This is done so that the **A102**fc will have a standard output mode equivalent to the **A101**fc. This type of output is sometimes called “Bayer 8.”

3.13.2 Customizable Formats and Modes

Format 7, Mode 0 and Format 7, Mode 1 are available on **A102fc** color cameras.

Format 7, Mode 0

Format 7, Mode 0 is used to enable and set up the area of interest (AOI) feature described in Section 3.6. Format 7, Mode 0 is parameterized by using the Format 7, Mode 0 control and status registers (see page 4-27).

When the camera is operating in Format 7, Mode 0, the frame rate can be adjusted by setting the number of bytes transmitted in each packet. The number of bytes per packet is set by the Bytes Per Packet field of the Bytes Per Packet control register.

The value that appears in the Max Bytes Per Packet field of the Packet Para Inquiry register will show the maximum allowed bytes per packet setting given the current AOI settings. When the bytes per packet is set to the maximum, the camera will transmit frames at its maximum specified rate. By default, the AOI is set to use the full sensor area and the bytes per packet is set to 4096.

If you set the bytes per packet to a value lower than the maximum, the camera will transmit frames at a lower rate. The rate is calculated by the formula:

$$\text{Frames/Sec.} = \frac{1}{\text{Packets per Frame} \times 125\ \mu s}$$

Keep in mind that when you lower the bytes per packet setting, the number of bytes needed to transmit a frame (the packets per frame) will increase. Due to limitations in the DCAM structure, a maximum of 4095 packets per frame is allowed. If you set the bytes per packet too low, the number of packets per frame will exceed the 4095 packet limit and the camera will not transmit frames properly.

When the camera is operating in Format 7, the Current Video Frame Rate control register is not used and has no effect on camera operation.

Color Codlings

In Format 7, Mode 0, the Mono 8, Raw 8, Raw 16, and YUV 4:2:2 color codlings are available.

When the **Mono 8** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs 8 bits per pixel and outputs only the Y component (brightness) of the YUV format.

When the **Raw 8** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs 8 bits per pixel and outputs the raw data for each pixel. The pixel data is not processed to account for the color filter. (This type of output is sometimes called “Bayer 8.”)

When the **Raw 16** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs 16 bits per pixel but only 12 bits are effective. The effective pixel data fills from the LSB and the unused bits are filled with zeros. Pixel data is stored in the PC memory in little Indian format, i.e., the low byte for each pixel is stored at the lower address and the high byte is stored at the neighboring higher address. The camera outputs raw data for each pixel. The pixel data is not processed to account for the color filter.

When the **YUV 4:2:2** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 0, the camera outputs image data in the YUV 4:2:2 format at an average of 16 bits per pixel.

When the camera is set for the Raw 16 or the YUV 4:2:2 color coding, the maximum frame rate at full resolution is 11.3 frames/s.

The Raw 8 and Raw 16 color codlings are defined in version 1.31 of the IIDC specification.

Color code definitions can very from camera model to camera model. This is especially true for older models of Basler cameras.

Format 7, Mode 1

Format 7, Mode 1 is very similar to Format 7, Mode 0 with the exception of the available color codlings and how the color codlings work.

Format 7, Mode 1 is parameterized by using the Format 7, Mode 1 control and status registers (see page 4-34).

Color Codlings

In Format 7, Mode 1, only the Mono 8 color coding is available and the color coding works differently than the Mono 8 color coding available in Format 7, Mode 0.

When the **Mono 8** ID is set in the Coding ID field of the Color Coding ID register for Format 7, Mode 1, the camera outputs 8 bits per pixel and outputs the raw data for each pixel. The pixel data is not processed to account for the color filter. (This type of output is sometimes called “Bayer 8.”)

This mode of operation is included on the **A102fc** for compatibility with versions 1.6 and below of the Basler BCAM 1394 driver software. These early versions of the BCAM software require a Mono 8 color coding that results in the output of raw pixel data.

3.14 Error Flags

A102f cameras support the following error flags:

- Error flags that indicate whether the current trigger, shutter, gain, brightness, and white balance settings are outside the specified range of allowed values. These error flags are set in the Trigger, Shutter, Gain, Brightness and White Balance fields of the Feature Control Error Status High register (see page 4-25).
- An error flag that indicates whether the current combination of the following settings is acceptable to the camera:
  - Video format
  - Mode
  - Frame rate
  - ISO speed

  This error flag is available for Format 2 only and is set in the VMode Error Status register (see page 4-18).
- An error flag that indicates whether the current combination of the following settings is acceptable to the camera:
  - Image position
  - Image size
  - Color coding ID
  - ISO speed

  This error flag is available for Format 7 only.

  If you are operating the camera in Format 7, Mode 0, the flag is set in the Error Flag 1 field of the Value Setting register for Format 7, Mode 0 (see page 4-33).

  If you are operating the camera in Format 7, Mode 1, the flag is set in the Error Flag 1 field of the Value Setting register for Format 7, Mode 1 (see page 4-40).
- An error flag that indicates whether the current bytes per packet setting is acceptable to the camera.

  This error flag is available for Format 7 only.

  If you are operating the camera in Format 7, Mode 0, the flag is set in the Error Flag 2 field of the Value Setting register for Format 7, Mode 0 (see page 4-33).

  If you are operating the camera in Format 7, Mode 1, the flag is set in the Error Flag 2 field of the Value Setting register for Format 7, Mode 1 (see page 4-40).

The error flag registers are defined in version 1.31 of the IIDC specification.

3.15 Configuration Sets and Memory Channels

A configuration set is a group of values that contains all of the register settings needed to control the camera. There are two basic types of configuration sets: the work configuration set and the factory configuration set.

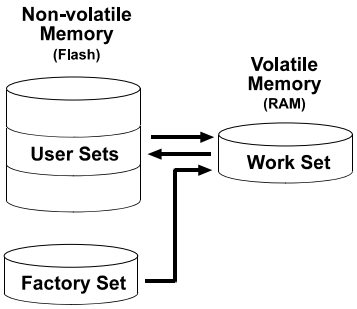

Figure 3-15: Configuration Sets

Work Configuration Set

The work configuration set contains the camera's current register settings and thus determines the camera's performance, that is, what your image currently looks like. When you change settings by writing to the camera's registers, you are making changes to the work configuration set. The work configuration set is located in the camera's volatile memory and the settings are lost if the camera is reset or if power is switched off. The work configuration set is usually just called the "work set" for short.

Factory Configuration Set

When a camera is manufactured, a test setup is performed on the camera and an optimized configuration is determined. The factory configuration set contains the camera's factory optimized configuration. The factory set is saved in a permanent file in the camera's non-volatile memory. The factory set can not be altered and since it is stored in non-volatile memory, it is not lost when the camera is reset or switched off. The factory configuration set is usually just called the "factory set" for short.

3.15.1 Saving Configuration Sets

As mentioned above, the work configuration set is stored in the camera's volatile memory and the settings are lost if the camera is reset or if power is switched off. **A102f** cameras can save the current work set values in the volatile memory to reserved areas in the camera's non-volatile memory called "memory channels." Configuration sets saved to memory channels in the non-volatile memory are not lost at reset or power off. There are three memory channels available for saving configuration sets - channel 1, channel 2 and channel 3. A configuration set saved in a memory channel is commonly referred to as a "user configuration set" or "user set."

Saving the current work set to one of the memory channels is a three step process:

1. Make changes to the camera's settings until the camera is operating in a manner that you would like to save.
2. Set the value of the Memory Save Channel control register (see page 4-18) to 1, 2, 3. This will select the channel were the configuration set will be saved.
3. Set the value of the Memory Save control register (see 4-17) to 1. When you set this value to 1, the camera will save the current register settings to the designated memory channel.

Saving a configuration set to one of the memory channels will overwrite any set that was previously saved to the selected channel.

3.15.2 Copying a Saved Configuration Set or the Factory Set into the Work Set

If you have saved one or more configuration sets to memory channels in the camera as described in Section 3.15.1, you can copy one of the saved sets from a memory channel into the camera's work set. When you do this, the copied set overwrites the parameters in the work set. Since the settings in the work set control the current operation of the camera, the settings from the copied set will now be controlling the camera.

To copy a saved configuration set from a memory channel into the work set:

1. Set the value in the Current Memory Channel control register (see page 4-18) to 1, 2 or 3. When you set the register, the configuration settings will be copied from the designated channel into the work set.

By default, the factory set is stored in memory channel 0. This is a protected memory channel and the factory settings in this channel can't be altered in any way. You can copy the factory configuration set into the work set if you desire.

To copy the factory set from memory channel 0 into the work set:

1. Set the value in the Current Memory Channel control register to 0. When you set the register, the factory configuration settings will be copied into the work set.

Copying a saved configuration set or the factory set into the work set is only allowed when the camera is idle, i.e., when it is not capturing images continuously and does not have a one shot capture pending.

Copying the factory set into the work set is a good course of action if you have grossly misadjusted the settings in the camera and you are not sure how to recover. The factory settings are optimized for use in typical situations and will provide good camera performance in most cases.

3.15.3 Designating a Startup Memory Channel

Whenever a camera is powered on or is reset, by default, it copies the factory set settings in memory channel 0 into the work set. **A102f** cameras have a "startup channel" feature that lets you change this behavior. The startup channel feature designates which memory channel will be used at power on or reset. For example, if the startup channel is designated as memory channel 2, the settings in memory channel 2 will be copied into the work set at power on or reset.

The startup channel feature on **A102f** cameras has been implemented as a smart feature. See Section 6.7.12 for more information on the startup channel smart feature.

You can only designate memory channel 1, 2 or 3 as the startup chanel if you have previously saved a configuration set into the designated channel. You cannot use an empty memory channel as the startup channel.

4 Configuring the Camera

A102f cameras are configured by setting status and control registers as described in the “1394-Based Digital Camera Specification” issued by the 1394 Trade Association. The specification is commonly referred to as the “DCAM standard” or the “IIDC” standard.” It is available at the 1394 Trade Association’s web site: www.1394ta.org. Except where noted, all registers conform to version 1.31 of the DCAM standard.

If you are creating your own driver to operate the camera, Sections 4.1 through 4.4 provide the basic information you need about the registers implemented in the camera along with some information about read/write capabilities and the image data format.

The DCAM standard also outlines a set of “Advanced Features” registers. These registers can be used to implement vendor unique features not defined in the standard. The Basler “Smart Features Framework” takes advantage of these registers to implement features such as a frame counter and test images. See Section 6 for more information.

The BCAM Driver

A fully functional driver is available for Basler IEEE 1394 cameras such as the **A102f**. The Basler BCAM 1394 Driver/Software Development Kit includes an API that allows a C++ programmer to easily integrate camera configuration and operating functions into your system control software.

The driver also includes a Windows® based viewer program that provides camera users with quick and simple tools for changing camera settings and viewing captured images.

The BCAM 1394 Driver/SDK comes with comprehensive documentation including a programmer’s guide and code samples. For more information, visit the Basler web site at: www.basler-vc.com.

4.1 Block Read and Write Capabilities

The camera supports block reads and block writes. If you do a single read or a block read, the camera will return a 0 for all non-existent registers. If you do a single write to a non-existent register or a block write that includes non-existent registers, the writes to non-existent registers will have no effect on camera operation.

Block reads or writes are limited to a payload of 32 quadlets.

4.2 Changing the Video Format setting

Whenever the Video Format setting is changed, you should also do the following:

If the Video Format is changed from Format 7 to Format 2, you should also check the Video Mode and the Video Frame Rate settings (see page 4-16). If necessary, change the Mode and Frame Rate settings so that they are compatible with Format 2.

If the Video Format is changed from Format 2 to Format 7, you should also check the Video Mode, the Image Position, the Image Size and the Bytes Per Packet settings (see pages 4-16 and 4-27). If necessary, change the Mode, Position, Size and Bytes per Packet settings so that they are compatible with Format 7.

4.3 Configuration ROM

The configuration ROM in the **A102f** is compliant with the DCAM specification V 1.31.

4.4 Implemented Standard Registers

This section includes a description of all DCAM standard registers implemented in the **A102f**.

4.4.1 Inquiry Registers

The base address for all inquiry registers is:

Bus ID, Node ID, FFFF F0F0 0000

In each inquiry register description, an “Offset from Base Address” is provided. This a byte offset from the above base address. The address of an inquiry register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

4.4.1.1 Initialize Inquiry Register

Register Name:		Camera Initialize
Offset from Base Address:		0x000
Field	**Bit**	**Description**
Initialize	0	If you set this bit to 1, the camera will reset itself, break any state lock, and re-initialize itself to the settings in the currently assigned startup memory channel (see Sections 3.15 and 6.7.12) . The bit is self cleared.
---	1 ... 31	Reserved

4.4.1.2 Inquiry Registers for Video Formats

Each bit in the video format inquiry register indicates the availability of a specific format.
0 = format not available 1 = format available

Register Name:		Video Format Inquiry		
Offset from Base Address:		0x100		
Field Name	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Format 0	0	VGA non-compressed format	0	0
Format 1	1	Super VGA non-compressed format (1)	0	0
Format 2	2	Super VGA non-compressed format (2)	1	1
Format x	3 ... 5	Reserved	---	---
Format 6	6	Still image format	0	0
Format 7	7	Partial image size format	1	1
---	8 ... 31	Reserved	---	---

4.4.1.3 Inquiry Registers for Video Modes

Each bit in the video mode inquiry register indicates the availability of a specific video format and mode combination (e.g., Format 0, Mode 0).

0 = not available 1 = available

Register Name:		Video Mode Inquiry for Format 2		
Offset from Base Address:		0x188		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Mode 0	0	1280 x 960, YUV 4:2:2, 16 bits/pixel	0	1
Mode 1	1	1280 x 960, RGB, 24 bits/pixel	0	0
Mode 2	2	1280 x 960, Y Mono, 8 bits/pixel	1	1
Mode 3	3	1600 x 1200, YUV 4:2:2, 16 bits/pixel	0	0
Mode 4	4	1600 x 1200, RGB, 24 bits/pixel	0	0
Mode 5	5	1600 x 1200, Y Mono, 8 bits/pixel	0	0
Mode 6	6	1280 x 960, Y Mono, 16 bits/pixel	1	0
Mode 7	7	1600 x 1200, Y Mono, 16 bits/pixel	0	0
---	8 ... 31	Reserved	---	---

Register Name:		Video Mode Inquiry for Format 7		
Offset from Base Address:		0x19C		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Mode 0	0	Format 7, Mode 0	1	1
Mode 1	1	Format 7, Mode 1	0	1
Mode 2	2	Format 7, Mode 2	0	0
Mode 3	3	Format 7, Mode 3	0	0
Mode 4	4	Format 7, Mode 4	0	0
Mode 5	5	Format 7, Mode 5	0	0
Mode 6	6	Format 7, Mode 6	0	0
Mode 7	7	Format 7, Mode 7	0	0
---	8 ... 31	Reserved	0	0

4.4.1.4 Inquiry Registers for Video Frame Rates

Each bit in the video frame rates inquiry register indicates the availability of a specific video format, mode, frame rate combination (e.g., Format 0, Mode 0, Frame Rate 0).

0 = format not available 1 = format available

Register Name:		Video Frame Rate Inquiry for Format 2, Mode 0		
Offset from Base Address:		0x240		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Frame Rate 0	0	1.875 fps standard frame rate	0	0
Frame Rate 1	1	3.75 fps standard frame rate	0	0
Frame Rate 2	2	7.5 fps standard frame rate	0	1
Frame Rate 3	3	15 fps standard frame rate	0	0
Frame Rate 4	4	30 fps standard frame rate	0	0
Frame Rate 5	5	60 fps standard frame rate	0	0
Frame Rate 6	6	Reserved	---	---
Frame Rate 7	7	Reserved	---	---
---	8 ... 31	Reserved	---	---

Register Name:		Video Frame Rate Inquiry for Format 2, Mode 2		
Offset from Base Address:		0x248		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Frame Rate 0	0	1.875 fps standard frame rate	0	0
Frame Rate 1	1	3.75 fps standard frame rate	0	0
Frame Rate 2	2	7.5 fps standard frame rate	0	0
Frame Rate 3	3	15 fps standard frame rate	1	1
Frame Rate 4	4	30 fps standard frame rate	0	0
Frame Rate 5	5	60 fps standard frame rate	0	0
Frame Rate 6	6	120 fps standard frame rate	0	0
Frame Rate 7	7	Reserved	---	---
----	8 ... 31	Reserved	---	---

Register Name:		Video Frame Rate Inquiry for Format 2, Mode 6		
Offset from Base Address:		0x258		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Frame Rate 0	0	1.875 fps standard frame rate	0	0
Frame Rate 1	1	3.75 fps standard frame rate	0	0
Frame Rate 2	2	7.5 fps standard frame rate	1	0
Frame Rate 3	3	15 fps standard frame rate	0	0
Frame Rate 4	4	30 fps standard frame rate	0	0
Frame Rate 5	5	60 fps standard frame rate	0	0
Frame Rate 6	6	Reserved	---	---
Frame Rate 7	7	Reserved	---	---
---	8 ... 31	Reserved	---	---

4.4.1.5 Inquiry Registers for Format 7 CSR Offsets

Register Name:		Video CSR Inquiry for Format 7, Mode 0
Offset from Base Address:		0x2E0
Field	**Bit**	**Description**
Mode 0	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the Format 7, Mode 0 Control and Status Register (CSR). (The A102f and A102fc support Format 7, Mode 0)

Register Name:		Video CSR Inquiry for Format 7, Mode 1
Offset from Base Address:		0x2E4
Field	**Bit**	**Description**
Mode 1	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the Format 7, Mode 1 Control and Status Register (CSR). (The A102fc supports Format 7, Mode 1)

4.4.1.6 Inquiry Register for Basic Functions

Each bit in the basic function inquiry register indicates the availability of a specific basic function.

0 = function not available 1 = function available

(The memory channel bits are an exception. Refer to the description below.)

Register Name:		Basic Function Inquiry		
Offset from Base Address:		0x400		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Advanced Feature Inq	0	Advanced (vendor unique) features availability	1	1
Vmode Error Status Inq	1	VMode Error Status register availability	1	1
Feature Control Error Status Register Inq	2	Feature Control Error Status register availability	1	1
Optional Function CSR Inq	3	Optional Function Control and Status register availability	1	1
---	4 ... 7	Reserved	---	
1394.b Mode Capability	8	IEEE 1394b capability	0	0
---	9 ... 15	Reserved	---	
Camera Power Ctrl.	16	Power on/off capability	0	0
---	17 ... 18	Reserved	---	
One Shot Inq	19	“One Shot” image capture mode availability	1	1
Multi Shot Inq	20	“Multi Shot” image capture mode availability	0	0
---	21 ... 27	Reserved	---	---
Memory Channels	28 ... 31	Indicates the maximum memory channel number available. If these bits are set to 0, the camera **does not** support memory channels.	3	3

4.4.1.7 Inquiry Register for Feature Presence

Each bit in the feature presence inquiry registers indicates the availability of a camera feature or optional function. Note that changing the video format or video mode may change the availability of a feature.

0 = feature not available 1 = feature available

Register Name:		Feature High Inquiry		
Offset from Base Address:		0x404		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Brightness	0	Brightness control availability	1	1
Auto Exposure	1	Auto exposure control availability	0	0
Sharpness	2	Sharpness control availability	0	0
White Balance	3	White balance control availability	0	1
Hue	4	Hue control availability	0	0
Saturation	5	Saturation control availability	0	0
Gamma	6	Gamma control availability	0	0
Shutter	7	Shutter speed control availability	1	1
Gain	8	Gain control availability	1	1
Iris	9	Iris control availability	0	0
Focus	10	Focus control availability	0	0
Temperature	11	Temperature control availability	0	0
Trigger	12	Trigger control availability	1	1
Trigger Delay Control	13	Trigger delay control availability	0	0
White Shading	14	White shading control availability	0	0
Frame Rate	15	Frame rate prioritization control availability	0	0
---	16 ... 31	Reserved	---	---

Register Name:		Feature Low Inquiry		
Offset from Base Address:		0x408		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Zoom	0	Zoom control availability	0	0
Pan	1	Pan control availability	0	0
Tilt	2	Tilt control availability	0	0
Optical Filter	3	Optical filter control availability	0	0
---	4 ... 15	Reserved	---	---
Capture Size	16	Format 6 capture size availability	0	0
Capture Quality	17	Format 6 capture quality availability	0	0
---	18 ... 31	Reserved	---	---

Register Name:		Optional Function Inquiry		
Offset from Base Address:		0x40C		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
---	0	Reserved	---	---
PIO	1	Parallel input/output control availability	1	1
SIO	2	Serial input/output control availability	0	0
Strobe Output	3	Strobe output control availability	1	1
---	4 ... 31	Reserved	---	---

Register Name:		Advanced Features Inquiry
Offset from Base Address:		0x480
Field	**Bit**	**Description**
Advanced Feature Quadlet Offset	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the advanced features Control and Status Registers (CSR). The A102f and A102fc support advanced (vendor unique) features.

Register Name:		PIO Control CSR Inquiry
Offset from Base Address:		0x484
Field	**Bit**	**Description**
PIO Control Quadlet Offset	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the PIO Control and Status Registers (CSR). The A102f and A102fc support PIO control.

Register Name:		Strobe Output CSR Inquiry
Offset from Base Address:		0x48C
Field	**Bit**	**Description**
Strobe Output Quadlet Offset	0 ... 31	Indicates the quadlet offset from the base address of the initial register space for the strobe output Control and Status Registers (CSR). The A102f and A102fc support strobe output control.

4.4.1.8 Inquiry Registers for Feature Elements

The feature element inquiry registers indicates the availability of elements, modes, maximum and minimum values for features. Note that changing the video format or video mode may change the availability of a feature element.

0 = element not available 1 = element available

Register Name:		Brightness Inquiry		
Offset from Base Address:		0x500		
Field	**Bit**	**Description**	**A102f Value**	**A102f Value**
Presence Inq	0	Brightness control feature is present	1	1
Abs Control Inq	1	Brightness can be set with an absolute value	0	0
---	2	Reserved	---	---
One Push Inq	3	One push auto mode is present	0	0
Read Out Inq	4	The brightness value can be read	1	1
On/Off Inq	5	Brightness control can be switched on/off	0	0
Auto Inq	6	A brightness auto control mode is present	0	0
Manual Inq	7	The brightness value can be set manually	1	1
Min Value	8 ... 19	Minimum value for brightness	0	0
Max Value	20 ... 31	Maximum value for brightness	255	255

Register Name:		White Balance Inquiry		
Offset from Base Address:		0x50C		
Field	**Bit**	**Description**	**A102f Value**	**A102f Value**
Presence Inq	0	White balance feature is present	0	1
Abs Control Inq	1	White balance can be set with an absolute value	0	0
---	2	Reserved	---	---
One Push Inq	3	One push auto mode is present	0	0
Read Out Inq	4	The white balance value can be read	0	1
On/Off Inq	5	White balance can be switched on/off	0	0
Auto Inq	6	A white balance auto control mode is present	0	0
Manual Inq	7	The white balance value can be set manually	0	1
Min Value	8 ... 19	Minimum value for white balance	---	16
Max Value	20 ... 31	Maximum value for balance	---	255

Register Name:		Shutter Inquiry		
Offset from Base Address:		0x51C		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Presence Inq	0	Shutter control feature is present	1	1
Abs Control Inq	1	Shutter can be set with an absolute value	0	0
---	2	Reserved	---	---
One Push Inq	3	One push auto mode is present	0	0
Read Out Inq	4	The shutter value can be read	1	1
On/Off Inq	5	Shutter control can be switched on/off	0	0
Auto Inq	6	A shutter auto control mode is present	0	0
Manual Inq	7	The shutter value can be set manually	1	1
Min Value	8 ... 19	Minimum value for shutter	1	1
Max Value	20 ... 31	Maximum value for shutter	In Format 2, depends on the format, mode and frame rate settings. In Format 7, the maximum is 4095.	

Register Name:		Gain Inquiry		
Offset from Base Address:		0x520		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Presence Inq	0	Gain control feature is present	1	1
Abs Control Inq	1	Gain can be set with an absolute value	0	0
---	2	Reserved	---	---
One Push Inq	3	One push auto mode is present	0	0
Read Out Inq	4	The gain value can be read	1	1
On/Off Inq	5	Gain control can be switched on/off	0	0
Auto Inq	6	A gain auto control mode is present	0	0
Manual Inq	7	The gain value can be set manually	1	1
Min Value	8 ... 19	Minimum value for gain	192	192
Max Value	20 ... 31	Maximum value for gain	When the camera is set for anything other than Mono 16 output: max = 1023 When the camera is set for Mono 16 output: max = 511	

Register Name:		Trigger Inquiry		
Offset from Base Address:		0x530		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Presence Inq	0	Trigger control feature is present	1	1
Abs Control Inq	1	Trigger can be set with an absolute value	0	0
---	2 ... 3	Reserved	---	---
Read Out Inq	4	The trigger value can be read	1	1
On/Off Inq	5	Trigger control can be switched on/off	1	1
Polarity Inq	6	The trigger input polarity can be changed	1	1
Value Read	7	The raw trigger input can be read	1	1
Trigger Source 0 Inq	8	Trigger source 0 is present (ID = 0)	1	1
Trigger Source 1 Inq	9	Trigger source 1 is present (ID = 1)	1	1
Trigger Source 2 Inq	10	Trigger source 2 is present (ID = 2)	1	1
Trigger Source 3 Inq	11	Trigger source 3 is present (ID = 3)	1	1
---	12 ... 14	Reserved	---	---
Software Trigger Inq	15	Software trigger is present (ID = 7)	1	1
Trigger Mode 0 Inq	16	Trigger mode 0 is present	1	1
Trigger Mode 1 Inq	17	Trigger mode 1 is present	1	1
Trigger Mode 2 Inq	18	Trigger mode 2 is present	0	0
Trigger Mode 3 Inq	19	Trigger mode 3 is present	0	0
Trigger Mode 4 Inq	20	Trigger mode 4 is present	0	0
Trigger Mode 5 Inq	21	Trigger mode 5 is present	0	0
---	22 ... 29	Reserved	---	---
Trigger Mode 14 Inq	30	Trigger mode 14 is present (Vendor unique trigger mode 0)	0	0
Trigger Mode 15 Inq	31	Trigger mode 15 is present (Vendor unique trigger mode 1)	0	0

4.4.2 Control and Status Registers

The base address for all camera control and status registers is:

Bus ID, Node ID, FFFF F0F0 0000

In each control and status register description, an “Offset from the Base Address” is provided. This a byte offset from the above base address. The address of a control and status register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

4.4.2.1 Control and Status Registers for Basic Camera Operation

Register Name:		Current Video Frame Rate / Revision
Offset from Base Address:		0x600
Field	**Bit**	**Description**
Frame Rate / Revision	0 ... 2	If a camera is set for video Format 2, this field sets the current video frame rate. 0 = frame rate 0 4 = frame rate 4 1 = frame rate 1 5 = frame rate 5 2 = frame rate 2 6 = frame rate 6 3 = frame rate 3 7 = frame rate 7 Default = 0 on the A102f and A102fc Check Sections 3.12 and 3.13 to determine the standard frame rates supported by the A102f and A102fc. If the camera is set for Format 7, the setting in this field is ignored. If the camera is set for Format 6, this field sets the current revision. (The A102f and A102fc do not support Format 6.)
---	3 ... 31	Reserved

Register Name:		Current Video Mode
Offset from Base Address:		0x604
Field	**Bit**	**Description**
Mode	0 ... 2	This field sets the current video mode. 0 = mode 0 4 = mode 4 1 = mode 1 5 = mode 5 2 = mode 2 6 = mode 6 3 = mode 3 7 = mode 7 Default = 0 on the A102f and A102fc Check Sections 3.12 and 3.13 to determine the video modes supported by the A102f and A102fc.
---	3 ... 31	Reserved

Register Name:		Current Video Format
Offset from Base Address:		0x608
Field	**Bit**	**Description**
Format	0 ... 2	This field sets the current video format. 0 = format 0 6 = format 6 1 = format 1 7 = format 7 2 = format 2 Default = 7 on the A102f and A102fc Check Sections 3.12 and 3.13 to determine the video formats supported on the A102f and A102fc.
---	3 ... 31	Reserved

Register Name:		ISO
Offset from Base Address:		0x60C
Field	**Bit**	**Description**
ISO Channel L	0 ... 3	Sets the isochronous channel number for video transmission for the legacy mode. 0 = channel 0 6 = channel 6 11 = channel 11 1 = channel 1 7 = channel 7 12 = channel 12 2 = channel 2 8 = channel 8 13 = channel 13 3 = channel 3 9 = channel 9 14 = channel 14 4 = channel 4 10 = channel 10 15 = channel 15 5 = channel 5 Default = 0 on the A102f and A102fc
---	4 ... 5	Reserved
Iso Speed L	6 ... 7	Sets the isochronous transmit speed code for the legacy mode. 0 = 100 M 1 = 200 M 2 = 400 M Default = 2 on the A102f and A102fc
---	8 ... 15	Reserved
Operation Mode	16	Sets the 1394 operation mode. 0 = Legacy 1 = 1394.b Default = 0 on the A102f and A102fc The A102f and A102fc do not support 1394b.
---	17	Reserved
Iso Channel B	18 ... 23	Not supported on the A102f or A102fc.
---	24 ... 28	Reserved
Iso Speed B	29 ... 31	Not supported on the A102f or A102fc.

Register Name:		ISO EN / Continuous Shot
Offset from Base Address:		0x614
Field	**Bit**	**Description**
Continuous Shot	0	When the camera is set for video Format 2 or Format 7, this field controls the “continuous shot” video transmission mode. 1 = start “continuous shot” transmission 0 = stop “continuous shot” transmission Default = 0 on the A102f and A102fc
---	1 ... 31	Reserved

Register Name:		Memory Save
Offset from Base Address:		0x618
Field	**Bit**	**Description**
Save	0	Writing a 1 to this field will cause the current settings in the work configuration set (see Section 3.15) to be saved to the memory channel specified in the Memory Save Channel register (see page 4-18). (This register self clears.)
---	1 ... 31	Reserved

Register Name:		One Shot / Multi Shot
Offset from Base Address:		0x61C
Field	**Bit**	**Description**
One Shot	0	When the camera is set for video Format 2 or Format 7, this field controls the “one shot” video transmission mode. 1 = transmit one frame of video data (Field is self cleared after transmission.) Default = 0 on the A102f and A102fc
Multi Shot	1	Multi shot is not supported on the A102f or A102fc.
---	2 ... 15	Reserved
Count Number	16 ... 31	The count number for multi shot is not supported on the A102f or A102fc.

Register Name:		Memory Save Channel
Offset from Base Address:		0x620
Field	**Bit**	**Description**
Save Channel	0 ... 3	When a 1 is written to the Memory Save register (see page 4-17), the current settings in the work configuration set (see Section 3.15) will be saved to the memory channel specified in this register. The valid values for this register are 1, 2 and 3.
---	4 ... 31	Reserved

Register Name:		Current Memory Channel
Offset from Base Address:		0x624
Field	**Bit**	**Description**
Current Channel	0	Writing a value to this field will cause the settings saved in the specified memory channel to be copied into the work configuration set (see Section 3.15). The valid values for writing to this register are 0, 1, 2 and 3. Reading the value from this register will indicate the last memory channel that was copied into the work configuration set.
---	1 ... 31	Reserved

Register Name:		VMode Error Status
Offset from Base Address:		0x628
Field	**Bit**	**Description**
Status	0	Used only when the camera is set for a standard format (not Format 7). This field will be updated each time the video format, mode, frame rate or ISO speed setting is changed. The value in this field indicates whether the current combination of video format, mode, frame rate and ISO speed settings is acceptable to the camera. 0 = the combination is OK, image capture can be started 1 = the combination is not OK, image capture can not be started This field is read only.
---	1 ... 31	Reserved

Register Name:		Software Trigger
Offset from Base Address:		0x62C
Field	**Bit**	**Description**
Trigger	0	When the Trigger Source field of the Trigger Mode register (see page 4-24) is set for a software trigger, this field controls the software trigger. 0 = reset the software trigger 1 = set the software trigger (If the Trigger Mode field of the Trigger Mode register is set to 0, this field will self clear.)
---	1 ... 31	Reserved

Register Name:		Data Depth	
Offset from Base Address:		0x630	
Field	**Bit**	**Description**	
Depth	0 ... 7	Indicates the effective depth of the data in the transmitted images. Depends on the current format and mode settings. Also depends on the Color Coding ID if the camera is set for Format 7. This field is read only.	
		Camera set for:	**Effective data depth indicated:**
		Mono 8 output	8 bits/pixel
		Mono 16 output	12 bits/pixel
		Raw 8 output	8 bits/pixel
		Raw 16 output	12 bits/pixel
		4:2:2 YUV output	8 bits/component
---	8 ... 31	Reserved	

4.4.2.2 Control and Status Registers for Features

Register Name:		Brightness
Offset from Base Address:		0x800
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the brightness control feature. The value will be 1 on A102f and A102fc cameras, indicating that brightness control is available. This field is read only.
Abs Control	1	Determines whether the brightness will be controlled by the Value field of this register or by the Absolute Value CSR for brightness. The value will be 0, indicating that brightness can only be controlled by the Value field of this register. Absolute value control is not available on A102f and A102fc cameras. This field is read only.
---	2 ... 4	Reserved
One Push	5	Sets “One Push” operation. The value will be 0, indicating that one push is not in operation. One push operation is not available on A102f and A102fc cameras. This field is read only.
On / Off	6	Sets whether brightness control is on or off. The value will be 1, indicating that brightness control is on. The brightness control feature can’t be switched off on A102f and A102fc cameras. This field is read only.
A / M Mode	7	Sets whether the camera is in automatic or manual brightness control mode. The value will be 0, indicating that brightness control is in manual mode. Automatic brightness control is not available on A102f and A102fc cameras. This field is read only.
---	8 ... 19	Reserved
Value	20 ... 31	Sets the brightness. The brightness value can range from 0 to 255. Default = 16 on the A102f Default = 32 on the A102fc If a camera is set for any output mode other than Mono 16, a brightness setting of around 8 will result in an offset of 0 in the digital values output for the pixels. An increase of 16 in the brightness setting will result in a positive offset of 1 in the digital values output for the pixels. If a camera is set for Mono 16 output, a brightness setting of around 0 will result in an offset of 0 in the digital values output for the pixels. An increase of 1 in the brightness setting will result in a positive offset of 1 in the digital values output for the pixels.

Register Name:		White Balance
Offset from Base Address:		0x80C
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the white balance control feature. The value will be 0 on A102f cameras, indicating that white balance control is not available. The value will be 1on A102fc cameras, indicating that white balance control is available. This field is read only.
Abs Control	1	Determines whether the white balance will be controlled by the Value field of this register or by the Absolute Value CSR for white balance. The value will be 0, indicating that white balance can only be controlled by the Value field of this register. Absolute value control is not available on A102f and A102fc cameras. This field is read only.
---	2 ... 4	Reserved
One Push	5	Sets “One Push” operation. The value will be 0, indicating that one push is not in operation. One push operation is not available on A102f and A102fc cameras. This field is read only.
On / Off	6	Sets whether white balance control is on or off. The value will be 1, indicating that white balance control is on. The white balance control feature can’t be switched off on A102f and A102fc cameras. This field is read only.
A / M Mode	7	Sets whether the camera is in automatic or manual white balance control mode. The value will be 0, indicating that white balance control is in manual mode. Automatic white balance control is not available on A102f and A102fc cameras. This field is read only.
Blue Value	8 ... 19	Adjusts the blue level in the captured images. The valid values for this field can range from 16 to 255, however, only settings from 64 to 255 should be used. When set to 96, blue will have the same “correction factor” as green. Settings less than 96 make the images less blue. Settings greater than 96 make the images more blue. Default = 151 on the A102fc
Red Value	20 ... 31	Adjusts the red level in the captured images. The valid values for this field can range from 16 to 255, however, only settings from 64 to 255 should be used. When set to 96, red will have the same “correction factor” as green. Settings less than 96 make the images less red. Settings greater than 96 make the images more red. Default = 122 on the A102fc

Register Name:		Shutter
Offset from Base Address:		0x81C
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the shutter control feature. The value will be 1on A102f and A102fc cameras, indicating that shutter control is available. This field is read only.
Abs Control	1	Determines whether the shutter will be controlled by the Value field of this register or by the Absolute Value CSR for the shutter. The value will be 0, indicating that the shutter can only be controlled by the Value field of this register. Absolute value control is not available on A102f and A102fc cameras. This field is read only.
---	2 ... 4	Reserved
One Push	5	Sets “One Push” operation. The value will be 0, indicating that one push is not in operation. One push operation is not available on A102f and A102fc cameras. This field is read only.
On / Off	6	Sets whether shutter control is on or off. The value will be 1, indicating that shutter control is on. The shutter control feature can’t be switched off on A102f and A102fc cameras. This field is read only.
A / M Mode	7	Sets whether the camera is in automatic or manual shutter control mode. The value will be 0, indicating that shutter control is in manual mode. Automatic shutter control is not available on A102f and A102fc cameras. This field is read only.
---	8 ... 19	Reserved
Value	20 ... 31	Sets the shutter value. The shutter value can range from 1 to 4095. Exposure time = (Shutter Value Setting) x (Shutter Time Base) Default = 500 on the A102f Default = 562 on the A102fc **Notes:** The shutter time base is normally 20 µs, but it can be adjusted by using the shutter time base smart feature. See Sections 3.2.1 and 6.7.13 for more information. On cameras with a firmware ID (see Section 1.1) lower than 27, an extra 38 µs was automatically added to the exposure time. On cameras with a firmware ID number of 27 and up, no time is added.

Register Name:		Gain
Offset from Base Address:		0x820
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the gain control feature. The value will be 1on A102f and A102fc cameras, indicating that gain control is available. This field is read only.
Abs Control	1	Determines whether the gain will be controlled by the Value field of this register or by the Absolute Value CSR for gain. The value will be 0, indicating that gain can only be controlled by the Value field of this register. Absolute value control is not available on A102f and A102fc cameras. This field is read only.
---	2 ... 4	Reserved
One Push	5	Sets “One Push” operation. The value will be 0, indicating that one push is not in operation. One push operation is not available on A102f and A102fc cameras. This field is read only.
On / Off	6	Sets whether gain control is on or off. The value will be 1, indicating that gain control is on. The gain control feature can’t be switched off on A102f and A102fc cameras. This field is read only.
A / M Mode	7	Sets whether the camera is in automatic or manual gain control mode. The value will be 0, indicating that gain control is in manual mode. Automatic gain control is not available on A102f and A102fc cameras. This field is read only.
---	8 ... 19	Reserved
Value	20 ... 31	Sets the gain. If the camera is set for any output mode other than Mono 16, the gain value can range from 192 to 1023. If the camera is set for Mono 16 output, the gain value can range from 192 to 511. A setting of 192 results in a gain of 0 dB (1x). A setting of 1023 results in a gain of 31 dB (35.5x). Default = 210 for the A102f Default = 224 for the A102fc

Register Name:		Trigger Mode
Offset from Base Address:		0x830
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the trigger mode control feature. The value will be 1on A102f and A102fc cameras, indicating that trigger mode control is available. This field is read only.
Abs Control	1	Determines whether the trigger mode will be controlled by the Value field of this register or by the Absolute Value CSR for the trigger mode. The value will be 0, indicating that the trigger mode can only be controlled by the Value field of this register. Absolute value control is not available on A102f and A102fc cameras. This field is read only.
---	2 ... 5	Reserved
On / Off	6	Sets whether trigger mode control is on or off. The value will be 1, indicating that trigger mode control is on. The trigger mode control feature can't be switched off on A102f and A102fc cameras. This field is read only.
Trigger Polarity	7	Sets the trigger polarity when the camera is using a hardware trigger. 0 = low active input 1 = high active input Default = 1 on the A102f and A102fc
Trigger Source	8 ... 10	Sets the trigger source. 0 = External trigger signal applied to physical input port 0 1 = External trigger signal applied to physical input port 1 2 = External trigger signal applied to physical input port 2 3 = External trigger signal applied to physical input port 3 7 = Software trigger Default = 0 on the A102f and A102fc
Trigger Value	11	Not used on the A102f or A102fc. This bit should be ignored.
Trigger Mode	12 ... 15	Sets the trigger mode. 0 = mode 0 (programmable mode) 1 = mode 1 (level mode) Default = 1 on the A102f and A102fc When an external trigger signal is used, mode 0 and mode 1 are both valid. When a software trigger is used, only mode 0 is valid. (See Section 3.2 for more information on exposure modes.)
---	16 ... 19	Reserved
Parameter	20 ... 31	Not used on the A102f or A102fc. These bits should be ignored.

4.4.2.3 Error Status Registers for Feature Control

As defined in the IIDC specification, each field in this register is an error or warning flag for the corresponding feature control register. If a bit = 1, the mode and/or value of the corresponding feature control register has an error or warning. If a bit = 0, no error or warning is present. Each field in this register will be updated whenever the corresponding feature control register is updated. If a bit = 1, we strongly recommend checking the corresponding control register.

On **A102f** and **A102fc** cameras, a feature's bit will become 1 when the feature's setting is outside the specified range of allowed settings, that is, the setting is lower than the allowed minimum or higher than the allowed maximum. If this situation occurs, **A102f** and **A102fc** cameras will continue image capture and you will see the undesired effects that result from the setting.

Register Name:		Feature Control Error Status High
Offset from Base Address:		0x640
Field	**Bit**	**Description**
Brightness	0	Indicates a brightness control error on the A102f or A102fc. 0 = no error present 1 = A setting in the brightness control register (see page 4-20) is outside of the allowed range This field is read only.
Auto Exposure	1	Not used on the A102f or A102fc. This bit should be ignored.
Sharpness	2	Not used on the A102f or A102fc. This bit should be ignored.
White Balance	3	Indicates a white balance control error on the A102fc. 0 = no error present 1 = A setting in the white balance control register (see page 4-21) is outside of the allowed range This field is read only.
Hue	4	Not used on the A102f or A102fc. This bit should be ignored.
Saturation	5	Not used on the A102f or A102fc. This bit should be ignored.
Gamma	6	Not used on the A102f or A102fc. This bit should be ignored.
Shutter	7	Indicates a shutter control error on the A102f or A102fc. 0 = no error present 1 = A setting in the shutter control register (see page 4-22) is outside of the allowed range This field is read only.
Gain	8	Indicates a gain control error on the A102f or A102fc. 0 = no error present 1 = A setting in the gain control register (see page 4-23) is outside of the allowed range This field is read only.
Iris	9	Not used on the A102f or A102fc. This bit should be ignored.
Focus	10	Not used on the A102f or A102fc. This bit should be ignored.
Temperature	11	Not used on the A102f or A102fc. This bit should be ignored.

Field	Bit	Description
Trigger	12	Indicates a trigger mode control error on the A102f or A102fc. 0 = no error present 1 = A setting in the trigger mode control register (see page 4-24) is outside of the allowed range This field is read only.
Trigger Delay	13	Not used on the A102f or A102fc. This bit should be ignored.
White Shading	14	Not used on the A102f or A102fc. This bit should be ignored.
Frame Rate	15	Not used on the A102f or A102fc. This bit should be ignored.
---	16 ... 31	Reserved

Register Name:		Feature Control Error Status Low
Offset from Base Address:		0x644
Field	**Bit**	**Description**
Zoom	0	Not used on the A102f or A102fc. This bit should be ignored.
Pan	1	Not used on the A102f or A102fc. This bit should be ignored.
Tilt	2	Not used on the A102f or A102fc. This bit should be ignored.
Optical Filter	3	Not used on the A102f or A102fc. This bit should be ignored.
---	4 ... 15	Reserved
Capture Size	16	Not used on the A102f or A102fc. This bit should be ignored.
Capture Quality	17	Not used on the A102f or A102fc. This bit should be ignored.
---	18 ... 31	Reserved

4.4.2.4 Control and Status Registers for Format 7, Mode 0

Format 7, Mode 0 is available on **A102f** and **A102fc** cameras. The base address for each Format 7, Mode 0 camera control register is:

Bus ID, Node ID, FFFF F1F0 0000

In each Format 7, Mode 0 register description, an “Offset from the Base Address” is provided. This is a byte offset from the above base address. The address of a Format 7, Mode 0 register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		Max Image Size Inquiry
Offset from Base Address:		0x000
Field	**Bit**	**Description**
Hmax	0 ... 15	Indicates the maximum horizontal image size in pixels. Hmax = 1392 on the A102f Hmax = 1388 on the A102fc
Vmax	16 ... 31	Indicates the maximum vertical image size in pixels. Vmax = 1040 on the A102f Vmax = 1038 on the A102fc

Register Name:		Unit Size Inquiry
Offset from Base Address:		0x004
Field	**Bit**	**Description**
Hunit	0 ... 15	Indicates the increment in columns for adjusting the area of interest width (see Section 3.6). For example, if the Hunit is 2, the width should be set in increments of 2. Hunit = 1 on the A102f Hunit = 2 on the A102fc
Vunit	16 ... 31	Indicates the increment in rows for adjusting the area of interest height (see Section 3.6). For example, if the Vunit is 1, the height should be set in increments of 1. Vunit = 1 on the A102f Vunit = 2 on the A102fc

Register Name:		Image Position
Offset from Base Address:		0x008
Field Name:	**Bit**	**Description**
Left	0 ... 15	Sets the left (starting) column of pixels for the area of interest (see Section 3.6). Default = 0 on the A102f and A102fc
Top	16 ... 31	Sets the top row of pixels for the area of interest (see Section 3.6). Default = 0 on the A102f and A102fc

Register Name:		Image Size
Offset from Base Address:		0x00C
Field	**Bit**	**Description**
Width	0 ... 15	Sets the width in columns for the area of interest (see Section 3.6). Default = 1392 on the A102f Default = 1388 on the A102fc
Height	16 ... 31	Sets the height in rows for the area of interest (see Section 3.6). Default = 1040 on the A102f Default = 1038 on the A102fc

Register Name:		Color Coding ID
Offset from Base Address:		0x010
Field	**Bit**	**Description**
Coding ID	0 ... 7	Sets the color coding. Valid color codings for Format 7 Mode 0 are listed in the Color Coding Inquiry register (see the next register description). Default = ID 0 on the A102f Default = ID 2 on the A102fc
---	8 ... 31	Reserved

Register Name:		Color Coding Inquiry		
Offset from Base Address:		0x014		
Field Name:	**Bit**	**Description**	**A102f Value ***	**A102fc Value ***
Mono 8	0	Y only, 8 bits, non-compressed (ID = 0)	1	1
4:1:1 YUV8	1	4:4:1 YUV, 8 bits/component, non-compressed (ID = 1)	0	0
4:2:2 YUV 8	2	4:2:2 YUV, 8 bits/component, non-compressed (ID = 2)	0	1
4:4:4 YUV 8	3	4:4:4 YUV, 8 bits/component , non-compressed (ID = 3)	0	0
RGB 8	4	RGB, 8 bits/component, non-compressed (ID = 4)	0	0
Mono 16	5	Y only, 16 bits, non-compressed (unsigned integer) (ID = 5)	1	0
RGB 16	6	RGB, 16 bits/component, non-compressed (unsigned integer) (ID = 6)	0	0
Signed Mono 16	7	Y only, 16 bits, non-compressed (signed integer) (ID = 7)	0	0
Signed RGB 16	8	RGB, 16 bits/component, non-compressed (signed integer) (ID = 8)	0	0
Raw 8	9	8 bit, raw data output from a color filter sensor (ID = 9)	0	1
Raw 16	10	16 bit, raw data output from a color filter sensor (ID = 10)	0	1
---	11 ... 31	Reserved	---	---

* If a bit is set to 0, the camera does not support this color coding ID in Format 7 Mode 0.
If a bit is set to 1, the camera supports this color coding ID in Format 7 Mode 0.

Register Name:		Pixel Number Inquiry
Offset from Base Address:		0x034
Field	**Bit**	**Description**
Pixels Per Frame	0 ... 31	Indicates the total number of pixels per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size register (see page 4-28).

Register Name:		Total Bytes High Inquiry
Offset from Base Address:		0x038
Field	**Bit**	**Description**
Bytes Per Frame High	0 ... 31	Indicates the higher quadlet of the total bytes of image data per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size and Color Coding ID registers (see page 4-28). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Total Bytes Low Inquiry
Offset from Base Address:		0x03C
Field	**Bit**	**Description**
Bytes Per Frame Low	0 ... 31	Indicates the lower quadlet of the total bytes of image data per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size and Color Coding ID registers (see page 4-28). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Packet Para Inquiry
Offset from Base Address:		0x040
Field	**Bit**	**Description**
Unit Bytes Per Packet	0 ... 15	Indicates the increment for setting the Bytes Per Packet field of the Bytes Per Packet register (see page 4-31). 4 = the increment for setting the bytes per packet on the A102f and A102fc.
Max Bytes Per Packet	16 ... 31	Indicates the maximum bytes per packet. 4096 = the maximum bytes per packet for the A102f and A102fc.

Register Name:		Bytes Per Packet
Offset from Base Address:		0x044
Field	**Bit**	**Description**
Bytes Per Packet	0 ... 15	Sets the number of bytes per packet (the packet size). **Note:** When you lower the bytes per packet setting, the number of packets needed to transmit a frame (the packets per frame) will increase. Due to limitations in the DCAM structure, a maximum of 4095 packets per frame is allowed. If you set the bytes per packet too low, the number of packets per frame will exceed the 4095 packet limit and the camera will not transmit frames properly.
Rec Byte Per Packet	16 ... 31	Indicates the minimum bytes per packet needed to achieve the highest possible frame rate with the current camera settings. The recommended bytes per packet field is updated whenever the Format 7 settings are changed.

Register Name:		Packets Per Frame Inquiry
Offset from Base Address:		0x048
Field	**Bit**	**Description**
Packets Per Frame	0 ... 31	Indicates the total packets per frame. The value in this register depends on settings in the Format 7, Mode 0 Image Size and Color Coding ID registers (see page 4-28) and on the setting in the Format 7, Mode 0 Bytes per Packet register (see above). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Unit Position Inquiry
Offset from Base Address:		0x04C
Field	**Bit**	**Description**
Hposunit	0 ... 15	Indicates the increment in columns for adjusting the area of interest starting column (see Section 3.6). For example, if the Hposunit is 2, the starting column should be adjusted in increments of 2. Hposunit = 1 for the A102f Hposunit = 2 for the A102fc
Vposunit	16 ... 31	Indicates the increment in rows for adjusting the area of interest starting row (see Section 3.6). For example, if the Vposunit is 1, the starting row should be adjusted in increments of 1. Vposunit = 1 for the A102f Vposunit = 2 for the A102fc

Register Name:		Frame Interval Inquiry
Offset from Base Address:		0x050
Field	**Bit**	**Description**
Frame Interval	0 ... 31	Indicates the current frame period in seconds. This value will be updated when you adjust any register that affects the frame period. The value in this register is a standard IEEE-754 single precision (32 bit) floating point number.

Register Name:		Data Depth Inquiry
Offset from Base Address:		0x054
Field	**Bit**	**Description**
Data Depth	0 ... 7	Indicates the effective depth of the data in the transmitted images. The value in this register depends on setting in the Format 7, Mode 0 Color Coding ID register (see page 4-28). This field is read only. **Color Coding ID setting:** — **Effective data depth indicated:** ID = 0 (Mono 8) — 8 bits/pixel ID = 2 (YUV 4:2:2) — 8 bits/component ID = 5 (Mono 16) — 12 bits/pixel ID = 9 (Raw 8) — 8 bits/pixel ID = 10 (Raw 16) — 12 bits/pixel
---	8 ... 31	Reserved

Register Name:		Color Filter ID
Offset from Base Address:		0x058
Field	**Bit**	**Description**
Filter ID	0 ... 7	Indicates the alignment of the camera's color filter to the current AOI. This field is valid for cameras equipped with an RGB primary color filter such as the A102fc. (See Sections 3.8 and 3.8.2.) **Value in this field:** — **Pixel color order:** 0 — RG/GB 1 — GB/RG 2 — GR/GB 3 — BG/GR
---	8 ... 31	Reserved

Register Name:		Value Setting
Offset from Base Address:		0x07C
Field	**Bit**	**Description**
Presence Inq	0	Indicates whether the fields in this register are valid. 0 = not valid 1 = valid The fields in this register are valid on the A102f and A102fc. The Presence Inq field is read only.
Setting 1	1	On the A102f and A102fc, this field is not relevant and should be ignored. (Updates to the register values monitored by this field are performed automatically.)
---	2 ... 7	Reserved
Error Flag 1	8	Indicates whether the combination of the values in the ISO Speed register and in the Format 7 Mode 0 Image Position, Image Size and Color Coding ID registers is acceptable. 0 = acceptable 1 = not acceptable and no image capture can be started
Error Flag 2	9	Indicates whether the value in the Bytes per Packet register is acceptable. 0 = acceptable 1 = not acceptable and no image capture can be started This field is updated whenever a value is written in the Bytes per Packet register.
---	10 ... 31	Reserved

4.4.2.5 Control and Status Registers for Format 7, Mode 1

Format 7, Mode 0 is available on **A102fc** cameras only. The base address for each Format 7, Mode 1 camera control register is:

Bus ID, Node ID, FFFF F1F0 0100

In each Format 7, Mode 0 register description, an “Offset from the Base Address” is provided. This is a byte offset from the above base address. The address of a Format 7, Mode 1 register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		Max Image Size Inquiry
Offset from Base Address:		0x000
Field	**Bit**	**Description**
Hmax	0 ... 15	Indicates the maximum horizontal image size in pixels. Hmax = 1388
Vmax	16 ... 31	Indicates the maximum vertical image size in pixels. Vmax = 1038

Register Name:		Unit Size Inquiry
Offset from Base Address:		0x004
Field	**Bit**	**Description**
Hunit	0 ... 15	Indicates the increment in columns for adjusting the area of interest width (see Section 3.6). For example, if the Hunit is 2, the width should be set in increments of 2. Hunit = 2
Vunit	16 ... 31	Indicates the increment in rows for adjusting the area of interest height (see Section 3.6). For example, if the Vunit is 1, the height should be set in increments of 1. Vunit = 2

Register Name:		Image Position
Offset from Base Address:		0x008
Field Name:	**Bit**	**Description**
Left	0 ... 15	Sets the left (starting) column of pixels for the area of interest (see Section 3.6). Default = 0
Top	16 ... 31	Sets the top row of pixels for the area of interest (see Section 3.6). Default = 0

Register Name:		Image Size
Offset from Base Address:		0x00C
Field	**Bit**	**Description**
Width	0 ... 15	Sets the width in columns for the area of interest (see Section 3.6). Default = 1388
Height	16 ... 31	Sets the height in rows for the area of interest (see Section 3.6). Default = 1038

Register Name:		Color Coding ID
Offset from Base Address:		0x010
Field	**Bit**	**Description**
Coding ID	0 ... 7	Sets the color coding. Valid color codings for Format 7 Mode 1 are listed in the Color Coding Inquiry register (see the next register description). Default = ID 0
---	8 ... 31	Reserved

Register Name:		Color Coding Inquiry	
Offset from Base Address:		0x014	
Field Name:	**Bit**	**Description**	**A102fc Value ***
Mono 8	0	8 bit raw value, non-compressed (ID = 0) This is a non-standard definition. When set to this color coding ID in Format 7 Mode 1, an A102fc will output the raw value for each pixel. The pixel data is not processed in any way to account for the color filter on the sensor. (This type of output is sometimes called “Bayer 8.”)	1
4:1:1 YUV8	1	4:4:1 YUV, 8 bits/component, non-compressed (ID = 1)	0
4:2:2 YUV 8	2	4:2:2 YUV, 8 bits/component, non-compressed (ID = 2)	0
4:4:4 YUV 8	3	4:4:4 YUV, 8 bits/component , non-compressed (ID = 3)	0
RGB 8	4	RGB, 8 bits/component, non-compressed (ID = 4)	0
Mono 16	5	Y only, 16 bits, non-compressed (unsigned integer) (ID = 5)	0
RGB 16	6	RGB, 16 bits/component, non-compressed (unsigned integer) (ID = 6)	0
Signed Mono 16	7	Y only, 16 bits, non-compressed (signed integer) (ID = 7)	0
Signed RGB 16	8	RGB, 16 bits/component, non-compressed (signed integer) (ID = 8)	0
Raw 8	9	8 bit, raw data output from a color filter sensor (ID = 9)	0
Raw 16	10	16 bit, raw data output from a color filter sensor (ID = 10)	0
---	11 ... 31	Reserved	---

* If a bit is set to 0, the camera does not support this color coding ID in Format 7 Mode 1.
If a bit is set to 1, the camera supports this color coding ID in Format 7 Mode 1.

Register Name:		Pixel Number Inquiry
Offset from Base Address:		0x034
Field	**Bit**	**Description**
Pixels Per Frame	0 ... 31	Indicates the total number of pixels per frame. The value in this register depends on settings in the Format 7, Mode 1 Image Size register (see page 4-35).

Register Name:		Total Bytes High Inquiry
Offset from Base Address:		0x038
Field	**Bit**	**Description**
Bytes Per Frame High	0 ... 31	Indicates the higher quadlet of the total bytes of image data per frame. The value in this register depends on settings in the Format 7, Mode 1 Image Size and Color Coding ID registers(see page 4-35). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Total Bytes Low Inquiry
Offset from Base Address:		0x03C
Field	**Bit**	**Description**
Bytes Per Frame Low	0 ... 31	Indicates the lower quadlet of the total bytes of image data per frame. The value in this register depends on settings in the Format 7 Mode 1 Image Size and Color Coding ID registers (see page 4-35). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Packet Para Inquiry
Offset from Base Address:		0x040
Field	**Bit**	**Description**
Unit Bytes Per Packet	0 ... 15	Indicates the increment for setting the Bytes per Packet field of the Bytes per Packet register (see page 4-31). 4 = the increment for setting the bytes per packet
Max Bytes Per Packet	16 ... 31	Indicates the maximum bytes per packet. 4096 = the maximum bytes per packet

Register Name:		Bytes Per Packet
Offset from Base Address:		0x044
Field	**Bit**	**Description**
Bytes Per Packet	0 ... 15	Sets the number of bytes per packet (the packet size). **Note:** When you lower the bytes per packet setting, the number of packets needed to transmit a frame (the packets per frame) will increase. Due to limitations in the DCAM structure, a maximum of 4095 packets per frame is allowed. If you set the bytes per packet too low, the number of packets per frame will exceed the 4095 packet limit and the camera will not transmit frames properly.
Rec Byte Per Packet	16 ... 31	Indicates the minimum bytes per packet needed to achieve the highest possible frame rate with the current camera settings. The recommended bytes per packet field is updated whenever the Format 7 settings are changed.

Register Name:		Packets Per Frame Inquiry
Offset from Base Address:		0x048
Field	**Bit**	**Description**
Packets Per Frame	0 ... 31	Indicates the total packets per frame. The value in this register depends on settings in the Format 7, Mode 1 Image Size and Color Coding ID registers (see page 4-35) and on the setting in the Bytes per Packet register (see above). The value in this register includes image data, padding bytes and any data added by enabled smart features (see Section 6).

Register Name:		Unit Position Inquiry
Offset from Base Address:		0x04C
Field	**Bit**	**Description**
Hposunit	0 ... 15	Indicates the increment in columns for adjusting the area of interest starting column (see Section 3.6). For example, if the Hposunit is 2, the starting column should be adjusted in increments of 2. Hposunit = 2
Vposunit	16 ... 31	Indicates the increment in rows for adjusting the area of interest starting row (see Section 3.6). For example, if the Vposunit is 1, the starting row should be adjusted in increments of 1. Vposunit = 2

Register Name:		Frame Interval Inquiry
Offset from Base Address:		0x050
Field	**Bit**	**Description**
Frame Interval	0 ... 31	Indicates the current frame period in seconds. This value will be updated when you adjust any register that affects the frame period. The value in this register is a standard IEEE-754 single precision (32 bit) floating point number.

Register Name:		Data Depth Inquiry
Offset from Base Address:		0x054
Field	**Bit**	**Description**
Data Depth	0 ... 7	Indicates the effective depth of the data in the transmitted images. The value in this register depends onthe setting in the Format 7, Mode 1 Color Coding ID register (see page 4-35). This field is read only. **Color Coding ID setting:** **Effective data depth indicated:** ID = 0 (Mono 8) 8 bits/pixel
---	8 ... 31	Reserved

Register Name:		Color Filter ID
Offset from Base Address:		0x058
Field	**Bit**	**Description**
Filter ID	0 ... 7	Indicates the alignment of the camera's color filter to the current AOI. This field is valid for cameras equipped with an RGB primary color filter such as the A102fc. (See Sections 3.8 and 3.8.2.) **Value in this field:** **Pixel color order:** 0 RG/GB 1 GB/RG 2 GR/GB 3 BG/GR
---	8 ... 31	Reserved

Register Name:		Value Setting
Offset from Base Address:		0x07C
Field	**Bit**	**Description**
Presence Inq	0	Indicates whether the fields in this register are valid. 0 = not valid 1 = valid The fields in this register are valid on the A102fc. The Presence Inq field is read only.
Setting 1	1	This field is not relevant and should be ignored. (Updates to the register values monitored by this field are performed automatically.)
---	2 ... 7	Reserved
Error Flag 1	8	Indicates whether the combination of the values in the ISO Speed register and in the Format 7 Mode 1 Image Position, Image Size and Color Coding ID registers is acceptable. 0 = acceptable 1 = not acceptable and no image capture can be started
Error Flag 2	9	Indicates whether the value in the Bytes per Packet register is acceptable. 0 = acceptable 1 = not acceptable and no image capture can be started This field is updated whenever a value is written in the Bytes per Packet register.
---	10 ... 31	Reserved

4.4.2.6 Control and Status Registers for the PIO Control Function

The base address for the PIO Control Function control and status registers is:

Bus ID, Node ID, FFFF F2F0 00C8

In each PIO register description, an “Offset the from Base Address” is provided. This a byte offset from the above base address. The address of a PIO register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		PIO Output
Offset from Base Address:		0x000
Field	**Bit**	**Description**
---	0 ... 27	Reserved
Port 3 Out	28	Sets the state of physical output port 3. 0 = low 1 = high
Port 2 Out	29	Sets the state of physical output port 2. 0 = low 1 = high
Port 1 Out	30	Sets the state of physical output port 1. 0 = low 1 = high
Port 0 Out	31	Sets the state of physical output port 0. 0 = low 1 = high

The PIO Output register can only set the state of a physical output port if that port is configured as “User Set” (see Section 6.7.11). For any output port not configured as user set, the bit setting in the PIO Output register will be ignored.

Register Name:		PIO Input
Offset from Base Address:		0x004
Field	**Bit**	**Description**
---	0 ... 27	Reserved
Port 3 In	28	Indicates the current state of physical input port 3. 0 = low 1 = high
Port 2 In	29	Indicates the current state of physical input port 2. 0 = low 1 = high
Port 1 In	30	Indicates the current state of physical input port 1. 0 = low 1 = high
Port 0 In	31	Indicates the current state of physical input port 0. 0 = low 1 = high

4.4.2.7 Control and Status Registers for the Strobe Signal Function

The base address for the Strobe Signal control and status registers is:

Bus ID, Node ID, FFFF F2F0 0300

In each Strobe Signal register description, an “Offset from the Base Address” is provided. This a byte offset from the above base address. The address of a strobe signal register equals the above base address plus the indicated offset.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		Strobe Control Inquiry		
Offset from Base Address:		0x000		
Field	**Bit**	**Description**	**A102f Value ***	**A102fc Value ***
Strobe 0 Inq	0	Presence of the Strobe 0 signal feature	1	1
Strobe 1 Inq	1	Presence of the Strobe 1 signal feature	1	1
Strobe 2 Inq	2	Presence of the Strobe 2 signal feature	1	1
Strobe 3 Inq	3	Presence of the Strobe 3 signal feature	1	1
---.	4 ... 31	Reserved	---	---

Register Name:		Strobe 0 Inquiry		
Offset from Base Address:		0x100		
Field	**Bit**	**Description**	**A102f Value ***	**A102fc Value ***
Presence Inq	0	Strobe 0 signal feature is present	1	1
---	1 ... 3	Reserved	---	---
Read Out Inq	4	The Strobe 0 value can be read	1	1
On/Off Inq	5	Strobe 0 control can be switched on/off	1	1
Polarity Inq	6	Strobe 0 polarity can be changed	1	1
---.	7	Reserved	---	---
Min Value	8 ... 19	Minimum value for Strobe 0 controls	0	0
Max Value	20 ... 31	Maximum value for Strobe 0 controls	4095	4095

* If a bit is set to 0, the camera does not support this feature
If a bit is set to 1, the camera supports this feature

Register Name:		Strobe 1 Inquiry		
Offset from Base Address:		0x104		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Same definitions and values as Strobe 0 Inq				

Register Name:		Strobe 2 Inquiry		
Offset from Base Address:		0x108		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Same definitions and values as Strobe 0 Inq				

Register Name:		Strobe 3 Inquiry		
Offset from Base Address:		0x10C		
Field	**Bit**	**Description**	**A102f Value**	**A102fc Value**
Same definitions and values as Strobe 0 Inq				

Register Name:		Strobe 0 Control
Offset from Base Address:		0x200
Field	**Bit**	**Description**
Presence Inq	0	Indicates the presence of the Strobe 0 signal control feature. 0 = not available 1 = available The Strobe 0 control feature is available on the A102f and A102fc. This field is read only.
---	1 ... 5	Reserved
On / Off	6	Sets whether the Strobe 0 signal is on or off. 0 = off 1 = on Default = 0 on the A102f and A102fc If this bit is 0, all other fields in this register are read only.
Signal Polarity	7	Sets the polarity of the Strobe 0 signal. 0 = low active 1 = high active Default = 1 on the A102f and A102fc
Delay Value	8 ... 19	Sets the delay value for the Strobe 0 signal (see Section 3.10). The delay value can range from 0 to 4095. Strobe 0 Delay = (Delay Value Setting) x (Strobe Delay Time Base) Default = 0 on the A102f and A102fc **Note:** The strobe delay time base is normally 1/1024 ms, but it can be adjusted by using the strobe time base smart feature. See Sections 3.10 and 6.7.14 for more information.
Duration Value	20 ... 31	Sets the duration value for the Strobe 0 signal. The duration value can range from 0 to 4095. Strobe 0 Duration = (Dur. Value Setting) x (Strobe Dur.Time Base) Default = 4095 on the A102f and A102fc **Note:** The strobe duration time base is normally 1/1024 ms, but it can be adjusted by using the strobe time base smart feature. See Sections 3.10 and 6.7.14 for more information.

Register Name:		Strobe 1 Control
Offset from Base Address:		0x204
Field	**Bit**	**Description**
Same definitions and values as Strobe 0 Control.		

Register Name:		Strobe 2 Control
Offset from Base Address:		0x208
Field	**Bit**	**Description**
Same definitions and values as Strobe 0 Control.		

Register Name:		Strobe 3 Control
Offset from Base Address:		0x20C
Field	**Bit**	**Description**
Same definitions and values as Strobe 0 Control.		

If a strobe signal is on, the signal will only be present on the associated output port if the output port is configured for “strobe.” For example, if the Strobe 0 signal is on, the signal will only be present on physical output port 0 if the port is configured for “strobe”. If the Strobe 1 signal is on, the signal will only be present on physical output port 1 if the port is configured for “strobe”. Etc.

See Section 6.7.11 for more information about configuring the output ports.

4.4.3 Advanced Features Registers

The base address for all advanced features registers is:

Bus ID, Node ID, FFFF F2F0 0000

The first eight quadlets of the advanced features register space is designated as the advanced features “Access Control Register” as described in the table below.

Values are stated in decimal format except when marked 0x. Values marked as 0x (e.g., 0x123) are in hexadecimal format. **Bit 0 in each register is the most significant bit.**

Register Name:		Special Features Access Control Register
Offset from Base Address:		0x000
Field	**Bit**	**Description**
Feature ID High	0 ... 31	On the A102f and A102fc, the value for Feature ID High field is: 0x0030 533B
Feature ID Low	32 ... 47	On the A102f and A102fc, the value for Feature ID Low field is: 0x73C3
0xF	48 ... 51	This value for this field always 0xF.
Time Out	52 ... 63	On the A102f and A102fc, the value for Time Out field is: 0x000

On the **A102f** and **A102fc**, all advanced features registers, including the Access Control register, have been made part of Basler’s Smart Features Framework (SFF). See Section 6 for a detailed explanation of using the SFF framework to access advanced features. (Section 6.5.1 contains specific information about using the Access Control register.)

5 Image Data Formats and Structures

5.1 Image Data Basics

Image data is transmitted as isochronous data packets according to the “1394 - based Digital Camera Specification” (DCAM) issued by the 1394 Trade Association (see the trade association’s web site: www.1394ta.org). The first packet of each frame is identified by a 1 in the sync bit of the packet header.

5.1.1 Pixel Transmission Sequence

Pixel data is transmitted from the camera in the following sequence on the A102f:

Row 0/Pixel 0, Row 0/Pixel 1, Row 0/Pixel 2 ... Row 0/Pixel 1390, Row 0/Pixel 1391

Row 1/Pixel 0, Row 1/Pixel 1, Row 1/Pixel 2 ... Row 1/Pixel 1390, Row 1/Pixel 1391

Row 2/Pixel 0, Row 2/Pixel 1, Row 2/Pixel 2 ... Row 2/Pixel 1390, Row 2/Pixel 1391

-
-

Row 1037/Pixel 0, Row 1037/Pixel 1, Row 1037/Pixel 2 ... Row 1037/ Pixel 1390, Row 1037/Pixel 1391

Row 1038/Pixel 0, Row 1038/Pixel 1, Row 1038/Pixel 2 ... Row 1038/ Pixel 1390, Row 1038/Pixel 1391

Row 1039/Pixel 0, Row 1039/Pixel 1, Row 1039/Pixel 2 ... Row 1039/ Pixel 1390, Row 1039/Pixel 1391

Pixel data is transmitted from the camera in the following sequence on the A102fc:

Row 0/Pixel 0, Row 0/Pixel 1, Row 0/Pixel 2 ... Row 0/Pixel 1386, Row 0/Pixel 1387

Row 1/Pixel 0, Row 1/Pixel 1, Row 1/Pixel 2 ... Row 1/Pixel 1386, Row 1/Pixel 1387

Row 2/Pixel 0, Row 2/Pixel 1, Row 2/Pixel 2 ... Row 2/Pixel 1386, Row 2/Pixel 1387

-
-

Row 1035/Pixel 0, Row 1035/Pixel 1, Row 1035/Pixel 2 ... Row 1035/ Pixel 1386, Row 1035/Pixel 1387

Row 1036/Pixel 0, Row 1036/Pixel 1, Row 1036/Pixel 2 ... Row 1036/ Pixel 1386, Row 1036/Pixel 1387

Row 1037/Pixel 0, Row 1037/Pixel 1, Row 1037/Pixel 2 ... Row 1037/ Pixel 1386, Row 1037/Pixel 1387

(These sequences assume that the camera is set for full resolution.)

5.2 Packet Payload Charts for Standard Format, Mode and Frame Rate Combinations on A102f Cameras

The following charts describe the packet payload for each standard format/mode/framerate combination available on the A102f or the A102fc. This information is especially useful when calculating a camera's bandwidth usage.

5.2.1 Format 2, Mode 0

(1280 x 960, YUV 4:2:2, 16 bits/pixel avg)

Frame Rate	**7.5 fps**
Lines per Packet	1/2
Pixels per Packet	640
Bytes per Packet	1280

5.2.2 Format 2, Mode 2

(1280 x 960, Y Mono, 8 bits/pixel)

Frame Rate	**15 fps**
Lines per Packet	2
Pixels per Packet	2560
Bytes per Packet	2560

5.2.3 Format 2, Mode 6

(1280 x 960, Y Mono, 16 bits/pixel)

Frame Rate	**7.5 fps**
Lines per Packet	1
Pixels per Packet	1280
Bytes per Packet	2560

5.3 Image Data Formats

5.3.1 Data Format with the Camera Set for YUV 4:2:2 Output

The table below describes how the data for a received frame will be ordered in the image buffer in your PC.

The following standards are used in the table:

P_0 = the first pixel transmitted by the camera

P_n = the last pixel transmitted by the camera

B_0 = the first byte in the buffer

B_m = the last byte in the buffer

Byte	Data
B_0	U value for P_0
B_1	Y value for P_0
B_2	V Value for P_0
B_3	Y value for P_1
B_4	U value for P_2
B_5	Y value for P_2
B_6	V Value for P_2
B_7	Y value for P_3
B_8	U value for P_4
B_9	Y value for P_4
B_{10}	V Value for P_4
B_{11}	Y value for P_5
•	•
•	•
•	•
B_{m-7}	U value for P_{n-3}
B_{m-6}	Y value for P_{n-3}
B_{m-5}	V Value for P_{n-3}
B_{m-4}	Y value for P_{n-2}
B_{m-3}	U value for P_{n-1}
B_{m-2}	Y value for P_{n-1}
B_{m-1}	V Value for P_{n-1}
B_m	Y value for P_n

5.3.2 Data Format with the Camera Set for Y Mono 8 Output

The table below describes how the data for a received frame will be ordered in the image buffer in your PC.

The following standards are used in the table:

P_0 = the first pixel transmitted by the camera

P_n = the last pixel transmitted by the camera

B_0 = the first byte in the buffer

B_m = the last byte in the buffer

Byte	Data
B_0	Y value for P_0
B_1	Y value for P_1
B_2	Y value for P_2
B_3	Y value for P_3
B_4	Y value for P_4
B_5	Y value for P_5
B_6	Y value for P_6
B_7	Y value for P_7
•	•
•	•
•	•
B_{m-3}	Y value for P_{n-3}
B_{m-2}	Y value for P_{n-2}
B_{m-1}	Y value for P_{n-1}
B_m	Y value for P_n

5.3.3 Data Format with the Camera Set for Y Mono 16 Output

The table below describes how the data for a received frame will be ordered in the image buffer in your PC.

The following standards are used in the table:

P_0 = the first pixel transmitted by the camera

P_n = the last pixel transmitted by the camera

B_0 = the first byte in the buffer

B_m = the last byte in the buffer

Byte	Data
B_0	Low byte of Y value for P_0
B_1	High byte of Y value for P_0
B_2	Low byte of Y value for P_1
B_3	High byte of Y value for P_1
B_4	Low byte of Y value for P_2
B_5	High byte of Y value for P_2
B_6	Low byte of Y value for P_3
B_7	High byte of Y value for P_3
B_8	Low byte of Y value for P_4
B_9	High byte of Y value for P_4
B_{10}	Low byte of Y value for P_5
B_{11}	High byte of Y value for P_5
•	•
•	•
•	•
B_{m-7}	Low byte of Y value for P_{n-3}
B_{m-6}	High byte of Y value for P_{n-3}
B_{m-5}	Low byte of Y value for P_{n-2}
B_{m-4}	High byte of Y value for P_{n-2}
B_{m-3}	Low byte of Y value for P_{n-1}
B_{m-2}	High byte of Y value for P_{n-1}
B_{m-1}	Low byte of Y value for P_n
B_m	High byte of Y value for P_n

As shown in the table above, when the camera is set for 16 bit output, data is placed in the image buffer in **little endian format**. (The DCAM standard specifies big endian format for 16 bit output, but we do not follow this recommendation. We use little endian format so that 16 bit data can be processed more effectively on little endian hardware such as Intel® processor based PCs.)

When the camera is set for 16 bit output, 16 bits of data will be transmitted for each pixel but only 12 bits are effective (see Section 3.9).

5.3.4 Data Format with the Camera Set for Raw 8 Output

The tables below describe how the data for the odd lines and for the even lines of a received frame will be ordered in the image buffer in your PC.

The following standards are used in the tables:

P_0 = the first pixel transmitted by the camera for a line

P_n = the last pixel transmitted by the camera a line

B_0 = the first byte of data for a line

B_m = the last byte of data for a line

For Filter ID = 0 (RG / GB)

Even Lines	
Byte	**Data**
B_0	Red value for P_0
B_1	Green value for P_1
B_2	Red value for P_2
B_3	Green value for P_3
B_4	Red value for P_4
B_5	Green value for P_5
•	•
•	•
•	•
B_{m-5}	Red value for P_{n-5}
B_{m-4}	Green value for P_{n-4}
B_{m-3}	Red value for P_{n-3}
B_{m-2}	Green value for P_{n-2}
B_{m-1}	Red value for P_{n-1}
B_m	Green value for P_n

Odd Lines	
Byte	**Data**
B_0	Green value for P_0
B_1	Blue value for P_1
B_2	Green value for P_2
B_3	Blue value for P_3
B_4	Green value for P_4
B_5	Blue value for P_5
•	•
•	•
•	•
B_{m-5}	Green value for P_{n-5}
B_{m-4}	Blue value for P_{n-4}
B_{m-3}	Green value for P_{n-3}
B_{m-2}	Blue value for P_{n-2}
B_{m-1}	Green value for P_{n-1}
B_m	Blue value for P_n

For Filter ID = 1 (GB / RG)

Even Lines	
Byte	**Data**
B_0	Green value for P_0
B_1	Blue value for P_1
B_2	Green value for P_2
B_3	Blue value for P_3
B_4	Green value for P_4
B_5	Blue value for P_5
•	•
•	•
•	•
B_{m-5}	Green value for P_{n-5}
B_{m-4}	Blue value for P_{n-4}
B_{m-3}	Green value for P_{n-3}
B_{m-2}	Blue value for P_{n-2}
B_{m-1}	Green value for P_{n-1}
B_m	Blue value for P_n

Odd Lines	
Byte	**Data**
B_0	Red value for P_0
B_1	Green value for P_1
B_2	Red value for P_2
B_3	Green value for P_3
B_4	Red value for P_4
B_5	Green value for P_5
•	•
•	•
•	•
B_{m-5}	Red value for P_{n-5}
B_{m-4}	Green value for P_{n-4}
B_{m-3}	Red value for P_{n-3}
B_{m-2}	Green value for P_{n-2}
B_{m-1}	Red value for P_{n-1}
B_m	Green value for P_n

For Filter ID = 2 (GR / BG)

Even Lines	
Byte	**Data**
B_0	Green value for P_0
B_1	Red value for P_1
B_2	Green value for P_2
B_3	Red value for P_3
B_4	Green value for P_4
B_5	Red value for P_5
•	•
•	•
•	•
B_{m-5}	Green value for P_{n-5}
B_{m-4}	Red value for P_{n-4}
B_{m-3}	Green value for P_{n-3}
B_{m-2}	Red value for P_{n-2}
B_{mn-1}	Green value for P_{n-1}
B_m	Red value for P_n

Odd Lines	
Byte	**Data**
B_0	Blue value for P_0
B_1	Green value for P_1
B_2	Blue value for P_2
B_3	Green value for P_3
B_4	Blue value for P_4
B_5	Green value for P_5
•	•
•	•
•	•
B_{m-5}	Blue value for P_{n-5}
B_{m-4}	Green value for P_{n-4}
B_{m-3}	Blue value for P_{n-3}
B_{m-2}	Green value for P_{n-2}
B_{m-1}	Blue value for P_{n-1}
B_m	Green value for P_n

For Filter ID = 3 (BG / GR)

Even Lines	
Byte	**Data**
B_0	Blue value for P_0
B_1	Green value for P_1
B_2	Blue value for P_2
B_3	Green value for P_3
B_4	Blue value for P_4
B_5	Green value for P_5
•	•
•	•
•	•
B_{m-5}	Blue value for P_{n-5}
B_{m-4}	Green value for P_{n-4}
B_{m-3}	Blue value for P_{n-3}
B_{m-2}	Green value for P_{n-2}
B_{m-1}	Blue value for P_{n-1}
B_m	Green value for P_n

Odd Lines	
Byte	**Data**
B_0	Green value for P_0
B_1	Red value for P_1
B_2	Green value for P_2
B_3	Red value for P_3
B_4	Green value for P_4
B_5	Red value for P_5
•	•
•	•
•	•
B_{m-5}	Green value for P_{n-5}
B_{m-4}	Red value for P_{n-4}
B_{m-3}	Green value for P_{n-3}
B_{m-2}	Red value for P_{n-2}
B_{m-1}	Green value for P_{n-1}
B_m	Red value for P_n

5.3.5 Data Format with the Camera Set for Raw 16 Output

The tables below describe how the data for the odd lines and for the even lines of a received frame will be ordered in the image buffer in your PC.

The following standards are used in the tables:

P_0 = the first pixel transmitted by the camera for a line

P_n = the last pixel transmitted by the camera a line

B_0 = the first byte of data for a line

B_m = the last byte of data for a line

For Filter ID = 0 (RG / GB)

Even Lines	
Byte	**Data**
B_0	Low byte of red value for P_0
B_1	High byte of red value for P_0
B_2	Low byte of green value for P_1
B_3	High byte of green value for P_1
B_4	Low byte of red value for P_2
B_5	High byte of red value for P_2
B_6	Low byte of green value for P_3
B_7	High byte of green value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of red value for P_{n-3}
B_{m-6}	High byte of red value for P_{n-3}
B_{m-5}	Low byte of green value for P_{n-2}
B_{m-4}	High byte of green value for P_{n-2}
B_{m-3}	Low byte of red value for P_{n-1}
B_{m-2}	High byte of red value for P_{n-1}
B_{m-1}	Low byte of green value for P_n
B_m	High byte of green value for P_n

Odd Lines	
Byte	**Data**
B_0	Low byte of green value for P_0
B_1	High byte of green value for P_0
B_2	Low byte of blue value for P_1
B_3	High byte of blue value for P_1
B_4	Low byte of green value for P_2
B_5	High byte of green value for P_2
B_6	Low byte of blue value for P_3
B_7	High byte of blue value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of green value for P_{n-3}
B_{m-6}	High byte of green value for P_{n-3}
B_{m-5}	Low byte of blue value for P_{n-2}
B_{m-4}	High byte of blue value for P_{n-2}
B_{m-3}	Low byte of green value for P_{n-1}
B_{m-2}	High byte of green value for P_{n-1}
B_{m-1}	Low byte of blue value for P_n
B_m	High byte of blue value for P_n

For Filter ID = 1 (GB / RG)

Even Lines	
Byte	**Data**
B_0	Low byte of green value for P_0
B_1	High byte of green value for P_0
B_2	Low byte of blue value for P_1
B_3	High byte of blue value for P_1
B_4	Low byte of green value for P_2
B_5	High byte of green value for P_2
B_6	Low byte of blue value for P_3
B_7	High byte of blue value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of green value for P_{n-3}
B_{m-6}	High byte of green value for P_{n-3}
B_{m-5}	Low byte of blue value for P_{n-2}
B_{m-4}	High byte of blue value for P_{n-2}
B_{m-3}	Low byte of green value for P_{n-1}
B_{m-2}	High byte of green value for P_{n-1}
B_{m-1}	Low byte of blue value for P_n
B_m	High byte of blue value for P_n

Odd Lines	
Byte	**Data**
B_0	Low byte of red value for P_0
B_1	High byte of red value for P_0
B_2	Low byte of green value for P_1
B_3	High byte of green value for P_1
B_4	Low byte of red value for P_2
B_5	High byte of red value for P_2
B_6	Low byte of green value for P_3
B_7	High byte of green value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of red value for P_{n-3}
B_{m-6}	High byte of red value for P_{n-3}
B_{m-5}	Low byte of green value for P_{n-2}
B_{m-4}	High byte of green value for P_{n-2}
B_{m-3}	Low byte of red value for P_{n-1}
B_{m-2}	High byte of red value for P_{n-1}
B_{m-1}	Low byte of green value for P_n
B_m	High byte of green value for P_n

For Filter ID = 2 (GR / BG)

Even Lines	
Byte	**Data**
B_0	Low byte of green value for P_0
B_1	High byte of green value for P_0
B_2	Low byte of red value for P_1
B_3	High byte of red value for P_1
B_4	Low byte of green value for P_2
B_5	High byte of green value for P_2
B_6	Low byte of red value for P_3
B_7	High byte of red value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of green value for P_{n-3}
B_{m-6}	High byte of green value for P_{n-3}
B_{m-5}	Low byte of red value for P_{n-2}
B_{m-4}	High byte of red value for P_{n-2}
B_{m-3}	Low byte of green value for P_{n-1}
B_{m-2}	High byte of green value for P_{n-1}
B_{m-1}	Low byte of red value for P_n
B_m	High byte of red value for P_n

Odd Lines	
Byte	**Data**
B_0	Low byte of blue value for P_0
B_1	High byte of blue value for P_0
B_2	Low byte of green value for P_1
B_3	High byte of green value for P_1
B_4	Low byte of blue value for P_2
B_5	High byte of blue value for P_2
B_6	Low byte of green value for P_3
B_7	High byte of green value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of blue value for P_{n-3}
B_{m-6}	High byte of blue value for P_{n-3}
B_{m-5}	Low byte of green value for P_{n-2}
B_{m-4}	High byte of green value for P_{n-2}
B_{m-3}	Low byte of blue value for P_{n-1}
B_{m-2}	High byte of blue value for P_{n-1}
B_{m-1}	Low byte of green value for P_n
B_m	High byte of green value for P_n

For Filter ID = 3 (BG / GR)

Even Lines	
Byte	**Data**
B_0	Low byte of blue value for P_0
B_1	High byte of blue value for P_0
B_2	Low byte of green value for P_1
B_3	High byte of green value for P_1
B_4	Low byte of blue value for P_2
B_5	High byte of blue value for P_2
B_6	Low byte of green value for P_3
B_7	High byte of green value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of blue value for P_{n-3}
B_{m-6}	High byte of blue value for P_{n-3}
B_{m-5}	Low byte of green value for P_{n-2}
B_{m-4}	High byte of green value for P_{n-2}
B_{m-3}	Low byte of blue value for P_{n-1}
B_{m-2}	High byte of blue value for P_{n-1}
B_{m-1}	Low byte of green value for P_n
B_m	High byte of green value for P_n

Odd Lines	
Byte	**Data**
B_0	Low byte of green value for P_0
B_1	High byte of green value for P_0
B_2	Low byte of red value for P_1
B_3	High byte of red value for P_1
B_4	Low byte of green value for P_2
B_5	High byte of green value for P_2
B_6	Low byte of red value for P_3
B_7	High byte of red value for P_3
•	•
•	•
•	•
B_{m-7}	Low byte of green value for P_{n-3}
B_{m-6}	High byte of green value for P_{n-3}
B_{m-5}	Low byte of red value for P_{n-2}
B_{m-4}	High byte of red value for P_{n-2}
B_{m-3}	Low byte of green value for P_{n-1}
B_{m-2}	High byte of green value for P_{n-1}
B_{m-1}	Low byte of red value for P_n
B_m	High byte of red value for P_n

As shown in the tables above, when the camera is set for 16 bit output, data is placed in the image buffer in **little endian format**. (The DCAM standard specifies big endian format for 16 bit output, but we do not follow this recommendation. We use little endian format so that 16 bit data can be processed more effectively on little endian hardware such as Intel® processor based PCs.)

When the camera is set for 16 bit output, 16 bits of data will be transmitted for each pixel but only 12 bits are effective (see Section 3.9).

5.4 Image Data Structure

5.4.1 Data Structure for a Y (Mono 8) or an R, G or B (Raw 8) Component

The data output for a Y (mono 8) component or an R, G or B (raw 8) component is 8 bit data of the “unsigned char” type. The range of data values for a Y mono component and the corresponding indicated signal levels are shown below.

This Data Value (Hexadecimal)	Indicates This Signal Level (Decimal)
0xFF	255
0xFE	254
●	●
●	●
●	●
0x01	1
0x00	0

5.4.2 Data Structure for a U or a V Component

The data output for a U or a V component is 8 bit data of the “straight binary” type. The range of data values for a U or a V component and the corresponding indicated signal levels are shown below.

This Data Value (Hexadecimal)	Indicates This Signal Level (Decimal)
0xFF	127
0xFE	126
●	●
●	●
●	●
0x81	1
0x80	0
0x7F	-1
●	●
●	●
●	●
0x01	-127
0x00	-128

The signal level of a U component or a V component can range from -128 to +127 (decimal). Notice that the data values have been arranged to represent the full signal level range.

5.4.3 Data Structure for a Y (Mono 16) or an R, G or B (Raw 16) Component

The data output for a Y (mono 16) component or an R, G or B (Raw 16) component is 16 bit data of the “unsigned short (little endian)” type. The range of data values for a Y mono component and the corresponding indicated signal levels are shown below.

This Data Value (Hexadecimal)	Indicates This Signal Level (Decimal)
0x0FFF	4095
0x0FFE	4094
•	•
•	•
•	•
0x0001	1
0x0000	0

Normally, the data values for a 16 bit component would range from 0x0000 to 0xFFFF. However, when an A102f or A102fc camera is set for 16 bit output, only 12 bits are effective. Therefore, the highest data value you will see is 0x0FFF indicating a signal level of 4095.

6 Smart Features and the Smart Features Framework

6.1 What are Smart Features

Smart features are features unique to Basler cameras. Test Images, the Cycle Time Stamp, and the CRC Checksum are examples of Basler smart features.

In some cases, enabling a smart feature will simply change the behavior of the camera. The Test Image feature is a good example of this type of smart feature. When the Test Image feature is enabled, the camera outputs a test image rather than a captured image.

When certain smart features are enabled, the camera actually develops some sort of information about each image that it acquires. In these cases, the information is added to each image as trailing data when the image is transmitted from the camera. Examples of this type of smart feature are the Cycle Time Stamp feature and the CRC Checksum. When the Cycle Time Stamp feature is enabled, after an image is captured, the camera determines when the acquisition occurred and develops a cycle time stamp for the image. And if the CRC Checksum feature is enabled, the camera calculates a checksum for the image. The cycle time stamp and checksum are added as trailing data to each image as the image is transmitted from the camera.

6.2 What is the Smart Features Framework

The first component of the Smart Features Framework (SFF) is a mechanism that allows you to enable and to parametrize smart features. This mechanism is essentially an extension of the register structure defined in the DCAM specification for use with “Advanced Features.” The SFF establishes a register for each smart feature. By setting bits within the register for a particular smart feature, you can enable the feature and control how the feature operates.

When certain smart features are enabled, the camera actually develops some sort of data about each image that it acquires. For example, when the Cycle Time Stamp feature is enabled, the camera creates a time stamp for each image based on when the image exposure started. In the cases where a smart feature develops some sort of data about a captured image, the smart feature’s data is added as trailing data to each image as the image is transmitted from the camera.

The SFF provides a mechanism for parsing the smart features data added to images transmitted out of the camera by assigning a unique identifier (GUID) to each smart feature. Whenever the camera adds data for a smart feature to an image, it includes the GUID for the smart feature as

part of the added data. The GUIDs are especially useful when you enable several smart features that add data to the image stream. The GUIDs make it possible to identify which portion of the added data is the result of each enabled smart feature. Refer to Sections 6.6 and 6.7 for detailed information about getting smart features results.

6.3 What do I Need to Use Smart Features

To use smart features you will need:

- A camera that supports smart features. Not all camera models support smart features. And with some camera models that do support smart features, you may find that older cameras may not support all available smart features or may not support smart features at all. Section 6.5 contains information about checking a camera to see if it supports smart features.
- A method of accessing the camera's DCAM register structure. We strongly recommend that you use the Basler BCAM 1394 Driver (v1.7 or higher) along with the Basler Smart Features Framework software to access the registers. (See Section 6.4 for more information about the SFF Software.)

We strongly recommend that you use the Basler BCAM 1394 driver. However, any driver that can get images in format 7 and that provides access to the DCAM registers can be used to work with smart features. If you do use a different driver, you can adapt the access techniques described in the SFF Software tutorial (see Section 6.4) to the driver you are using.

You should be aware that drivers other than the Basler BCAM driver have not been tested with smart features.

6.4 What is the Smart Features Framework Software?

A Smart Features Framework Software (SFF Software) package is available from Basler technical support. The SFF Software has two major components:

- An SFF Viewer. The viewer is a Windows® based tool that allows you to easily enable and disable smart features, parameterize the camera, capture and view images, and view smart features results.
- An SFF Tutorial. The tutorial explains how to access the cameras smart features from within your own applications. The tutorial is based on the assumption that you are using the Basler BCAM 1394 driver with your camera.

The SFF Viewer will only work on PCs that have the BCAM driver v1.7 or higher installed.

6.5 Enabling and Parameterizing Smart Features

The camera provides a control and status register (CSR) for each smart feature (see Sect 6.7 for details of each feature and its CSR). To enable and parameterize a smart feature, the following steps must be performed:

1. Check to see if the camera supports smart features.
2. Ask the camera for the address of the CSR for the desired smart feature.
3. Enable and parameterize the desired smart features.

The next two sections describe steps 1 and 2. The layout of the registers used to enable and parameterize the smart features is described in section 6.7.

6.5.1 Checking to see if the Camera Supports Smart Features

Smart features are vendor unique. Such features are referred to in the 1394 Trade Association DCAM standard as advanced features. The DCAM standard specifies how vendors should implement advanced features. According to the standard, advanced features must be unlocked (that is, enabled) by writing an advanced features set identifier (Feature ID) and a time-out value to the Advanced Features Access Control Register. The Feature ID associated with Basler smart features is 0x0030 533B 73C3. From the point of view of the DCAM standard, smart features are a set of advanced DCAM features.

For Basler cameras, unlocking advanced features is not strictly necessary because any implemented smart features are always available. However, the unlock mechanism is also used to check to see if a camera supports vendor unique features such as smart features. If a device doesn't recognize a Feature ID written to the Access Control Register, a value of 0xFFFF FFFF FFFF FFFF will be read back from the ACR. This value indicates that the device does not implement the feature set associated with that Feature ID.

Assuming that the address of the Advanced Features Access Control Register is 0xFFFF F2F0 0000, perform the following steps to see if a camera is smart features capable:

1. Write the quadlet data 0x0030 533B to 0xFFFF F2F0 0000
2. Write quadlet data 0x73C3 F000* to 0xFFFF F2F0 0004
3. Read quadlet data from 0xFFFF F2F0 0000 and 0xFFFF F2F0 0004. If at least one of the read operations returns a value that is not equal to 0xFFFF FFFF, the camera supports smart features. If both read operations return 0xFFFF FFFF, the camera does not support smart features.

Note that instead of performing two single quadlet write operations, a block write can be performed.

* The last three zeros in this quadlet represent a timeout value. When the timeout value is "000" as it is on the A102f, it means that advanced features are always available.

6.5.2 Determining the Address of a Smart Feature's CSR

The control and status register (CSR) for each smart feature is identified by a 128 bit Globally Unique Identifier (GUID). GUIDs are also known as UUIDs (Universal Unique Identifier).

A GUID consists of:

- One 32 bit number (D1)
- Two 16 bit numbers (D2, D3)
- A sequence of 8 bytes (D4[0] - D4[7])

GUID example:

CA8A916A	-	14A4	-	4D8E	-	BBC9	-	93DF50495C16
(D1)		(D2)		(D3)		(D4[0] - D4[1])		(D4[2] - D4[7])

Section 6.7 describes the standard smart features available on **A102f** cameras. Each smart feature description includes the GUID assigned to the feature's CSR.

To determine the starting address of a smart feature's CSR, the feature's CSR GUID must be written to the Smart Features Inquiry register. The Smart Features Inquiry register's offset relative to the Advanced Features Access Control Register is 0x10. If the camera recognizes the GUID as the CSR GUID for an implemented smart feature, the address of CSR for the feature can be read from the Smart Features Address Register at offset 0x20. If the feature isn't supported by the device, a value of 0x0 will be read from the Smart Features Address Register.

Smart Features Inquiry Register Layout

	Bit			
Offset	0-7	8-15	16-23	24-31
10h	D1			
14h	D3		D2	
18h	D4[3]	D4[2]	D4[1]	D4[0]
1ch	D4[7]	D4[6]	D4[5]	D4[4]

Smart Features Address Register Layout

	Bit			
Offset	0-7	8-15	16-23	24-31
20h	Address Low			
24h	Address High			

Example

Determine the address of the “CRC Checksum” smart feature which has a CSR GUID of:

3B34004E - 1B84 - 11D8 - 83B3 - 00105A5BAE55

D1: 0x3B34 004E

D2: 0x1B84

D3: 0x11D8

D4[0]: 0x83

D4[1]: 0xB3

D4[2]: 0x00

D4[3]: 0x10

D4[4]: 0x5A

D4[5]: 0x5B

D4[6]: 0xAE

D4[7]: 0x55

Step 1: Write the CSR GUID to the Smart Features Inquiry Register

Assuming that the address for the Access Control Register is 0xFFFF F2F0 0000, perform the following quadlet write operations to the Smart Features Inquiry Register

a. Write quadlet data 0x3B34 004E to 0xFFFF F2F0 0010 (D1)

b. Write quadlet data 0x11D8 1B84 to 0xFFFF F2F0 0014 (D3 | D2)

c. Write quadlet data 0x1000 B383 to 0xFFFF F2F0 0018 (D4[3] | D[0])

d. Write quadlet data 0x55AE 5B5A to 0xFFFF F2F0 001C (D4[7] | D[4])

Instead of performing four quadlet write operations, one block write operation can be performed.

Step 2: Read the start address for the smart feature from the Smart Features Address register

a. Read quadlet data from 0xFFFF F2F0 0020 (Address Low)

b. Read quadlet data from 0xFFFF F2F0 0024 (Address High)

If both Address Low and Address High return zero, the camera doesn’t support the CRC checksum feature. Assuming the read operations yielded Address Low = 0xF2F0 0038 and Address High = 0x0000 FFFF, the CRC Checksum feature CSR’s address is 0xFFFF F2F0 0038.

6.5.3 Enabling and Parameterizing a Smart Feature

Once you have determined the starting address of the control and status register (CSR) for your desired smart feature, you are ready to enable and parameterize the feature by setting bits within the CSR.

Section 6.7 describes the standard smart features available on **A102f** cameras. Each smart features description includes an explanation of what the feature does and an explanation of the parameters associated with the feature. The descriptions also include a detailed layout of how the bits contained within the feature's CSR relate to the parameters for the feature. After reading the description of your desired smart feature, you can enable and parameterize the feature by setting the appropriate bits within the CSR.

6.6 Getting Smart Features Results

In many cases, activating a smart feature results in additional data that must be transmitted by the camera, i.e., the results of the smart feature. The results of a smart feature will be appended to the image data so that each frame contains both image data and smart features results.

Before using any of the smart features that add information to the image data, the extended data stream feature must be enabled. The extended data stream is in itself a smart feature. When the extended data stream feature is enabled, information such as the height of the image, the width of the image, and the AOI size is added to each image's basic pixel data. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The extended data stream feature and any other smart features which add information to the image data stream will only work when the camera is set for video format 7. For other video formats, enabling the extended data stream feature or any of the other smart features that normally add data to the image stream does not affect the image data stream; the camera only sends the basic image data without any added information.

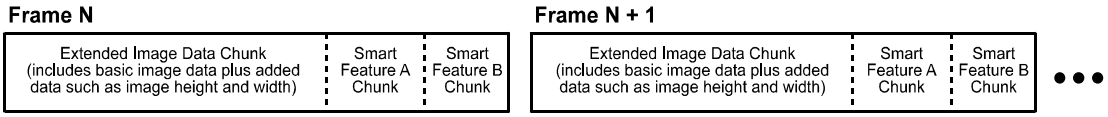

Figure 6-1: Image Data Stream with Smart Features Enabled

As illustrated in Figure 6-1, when smart features are enabled, each image frame consists of "chunks." For example, the frame may include a chunk which contains the extended image data (the basic image data plus the added height, width, etc. information), a chunk which contains the results for the frame counter smart feature, a chunk which contains the results for the cycle time stamp smart feature, etc. Table 6-1 describes the general structure of a chunk.

Position	Name	Description
0	Data [K Bytes]	The data that the chunk is transporting.
K	Chunk GUID [16 Bytes]	Identifies the type of chunk and the smart feature associated with the chunk. (Note that a smart feature's chuck GUID is not the same as its CSR GUID.)
K+16	Length [4 Bytes]	The chunk's total length in bytes.
K+20	Inverted Length [4 Bytes]	The bitwise complement of the length.

Table 6-1: General Structure of a Chunk

Each chunk ends with a four byte unsigned integer indicating the length of the chunk and four bytes which indicate the bitwise complement of the length. Transferring both the chunk length and the bitwise complement of the length serves as a mechanism to detect transmission errors. If the last four bytes of a chunk aren't the bitwise complement of the preceding four bytes, the chunk's length information isn't valid and this indicates that a transmission error occurred.

There are different types of chunks, for example, the chunk that is added when the cycle time stamp smart feature is enabled and the chunk that is added when the frame counter smart feature is enabled. Although most chunks follow the general structure described in Table 6-1, each type of chunk has unique aspects to its layout. To allow you to distinguish between the chunks, each chunk carries a “chunk GUID”. The GUID for each chunk is transferred just before the chunk’s length information. If you look through the descriptions of the smart features in Section 6.7, you will notice that for smart features which add a chunk to the image data stream, there is a description of the layout of the chunk and the chunk GUID associated with the chunk.

A chunk’s length field contains the chunk’s total length in bytes. The GUID, the length, and the inverted length are included as part of the total chunk length.

By appending length information and a chunk GUID to each chunk, the camera sends a self-describing data stream and allows easy navigation through the individual chunks that make up a complete image data frame.

Don’t confuse CSR GUIDs with chunk GUIDs:

- Each smart feature has a control and status register (CSR) associated with it and each CSR has a unique “CSR GUID” assigned to the register. The CSR GUIDs are used to help you keep track of which CSR is associated with each smart feature.
- Any smart feature that adds a “chunk” of data to the image data stream also has a unique “chunk GUID” assigned to the feature. The chunk GUID will be included the chunk of data that a smart feature adds to the image data. The chunk GUIDs let you determine which smart feature is associated with each added chunk in the image data stream.

The CRC Checksum is an exception to the general structure of a chunk. See Section 6.7.5 for more information.

6.6.1 How Big a Buffer Do I Need?

When smart features that add data to the image are enabled, the size of each transmitted frame will be larger than you would normally expect for a frame which contains only image data. To determine the size of the buffer that you will need to hold an image with appended smart features data, check the Total Bytes High Inquiry and Total Bytes Low Inquiry registers of the Format 7 mode you are currently using. Make sure to check these registers after all smart features have been enabled and all other settings affecting the image size have been completed. The size information in these fields will allow you to properly set up buffers to receive the transmitted images.

6.7 Smart Features on the A102f

6.7.1 Extended Data Stream

The extended data stream feature has two functions:

- When it is enabled, information such as image height, image width, and AOI size is added to the basic pixel data for each image.
- It must be enabled before you can use any other smart feature that adds information to the image data stream.

With the extended data stream feature enabled, the basic pixel data for each image and the added information such as the image height and width are included in an “extended data chunk”. Refer to the extended data chunk layout below for a complete description of the information included in the extended data chunk.

The extended data stream feature must be enabled in order to use any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The extended data stream feature and any other smart features which add information to the image data stream will only work when the camera is set for video format 7.

Control and Status Register for the Extended Data Stream Feature

Name	Extended Data Stream	
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID	4E7ABCB0 - 1B84 - 11D8 - 9651 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
----	[1 ... 30]	Reserved
Enable (Read / write)	[31]	Enable / Disable this feature 0: Disable 1: Enable

Extended Data Chunk Layout

Position	**Name**	**Description**
0	Pixel Data [K Bytes]	The pixel data from the captured image
K	Gap [M Bytes]	For technical reasons, there might be a gap between the pixel data and the other data in the extended image data.

K + M	Stride [4 Bytes]	Signed integer. Indicates the number of bytes needed to advance from the beginning of one row in an image to the beginning of the next row.
K + M + 4	Reserved [3 Bytes]	-----
K + M + 7	Data Depth [1 Byte]	Effective data depth in bits of the pixels in the image.
K + M + 8	Top [2 Bytes]	Y coordinate of the top left corner of the current area of interest (AOI).
K + M + 10	Left [2 Bytes]	X coordinate of the top left corner of the current AOI.
K + M + 12	Height [2 Bytes]	Height in pixels of the current AOI.
K + M + 14	Width [2 Bytes]	Width in pixels of the current AOI.
K + M + 16	Reserved [3 Bytes]	-----
K + M + 19	Color Coding ID [1 Byte]	Color coding ID which describes the pixel data format. See Sections 3.12.2 and 3.13.2 and pages 4-28 and 4-29.
K + M + 20	Reserved [3 Bytes]	-----
K + M + 23	Color Filter ID [1 Byte]	For color cameras, describes the orientation of the color filter to the current AOI. See Section 3.8.2 and page 4-32.
K + M + 24	Chunk GUID [16 Bytes]	94ED7C88 - 1C0F - 11D8 - 82E0 - 00105A5BAE55
K + M + 40	Chunk Length [4 Bytes]	This chunk's total length in bytes.
K + M + 44	Inverted Chunk Length [4 Bytes]	The bitwise complement of the chunk length.

6.7.2 Frame Counter

The frame counter feature numbers images sequentially as they are captured. The counter starts at 0 and wraps at 4294967296. The counter increments by one for each captured frame. Whenever the camera is powered off, the counter will reset to 0.

Note that if the camera is in continuous shot mode and continuous capture is stopped, up to two numbers in the counting sequence may be skipped. This happens due to the internal image buffering scheme used in the camera.

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the frame counter feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The frame counter feature will only work when the camera is set for video format 7.

Control and Status Register for the Frame Counter Feature

Name	Frame Counter	
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID	4433C4A4 - 1B84 - 11D8 - 86B2 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
----	[1 ... 30]	Reserved
Enable (Read / write)	[31]	Enable / Disable this feature 0: Disable 1: Enable

Frame Counter Chunk Layout

Position	**Name**	**Description**
0	Counter [4 Bytes]	The frame counter.
4	Chunk GUID [16 Bytes]	8C5DB844 - 1C0F - 11D8 - 965F - 00105A5BAE55
20	Chunk Length [4 bytes]	This chunk’s total length in bytes.
24	Inverted Chunk Length [4 bytes]	The bitwise complement of the chunk length.

6.7.3 Cycle Time Stamp

The cycle time stamp feature adds a chunk to each image frame containing the value of the counters for the IEEE 1394 bus cycle timer. The counters are sampled at the start of exposure of each image.

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the cycle time stamp feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The cycle time stamp feature will only work when the camera is set for video format 7.

Control and Status Register for the Cycle Time Stamp Feature

Name	Cycle Time Stamp	
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID	5590D58E - 1B84 - 11D8 - 8447 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
----	[1 ... 30]	Reserved
Enable (Read / write)	[31]	Enable / Disable this feature 0: Disable 1: Enable

Cycle Time Stamp Chunk Layout

Position	**Name**	**Description**		
0	Cycle Time Stamp [4 Bytes]	**Field**	**Bit**	**Description**
		Second Count	[0 ... 6]	Counts the seconds. Wraps to zero after 127 seconds.
		Cycle Count	[7 ... 19]	Counts the 125 µs isochronous bus cycles. Wraps to zero after counting to 7999.
		Cycle Offset	[20 ... 31]	Counts at 24.576 MHz and wraps to zero after counting to 3071 (resulting in a 125 µs cycle)
4	Chunk GUID [16 Bytes]	994DD430 - 1C0F - 11D8 - 8F6B - 00105A5BAE55		
20	Chunk Length [4 Bytes]	This chunk’s total length in bytes.		
24	Inverted Chunk Length [4 Bytes]	The bitwise complement of the chunk length.		

6.7.4 DCAM Values

The DCAM values feature adds a chunk to each image frame containing the current settings for some standard DCAM features. The settings are sampled at the start of exposure of each image.

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the DCAM values feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The DCAM values feature will only work when the camera is set for video format 7.

Control and Status Register for the DCAM Values Feature

Name	DCAM Values	
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID	494DE528 - 1B84 - 11D8 - 8A0C - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
----	[1 ... 30]	Reserved
Enable (Read / write)	[31]	Enable / Disable this feature 0: Disable 1: Enable

DCAM Values Chunk Layout

Position	Name	Description		
0	Gain CSR [4 Bytes]	Content of the DCAM Gain CSR		
		Field	**Bit**	**Description**
		Presence Inq	[0]	Presence of this feature If 0, the DCAM feature is not available and all of its values should be ignored
		Abs Control	[1]	Absolute control mode If 1, the DCAM feature is in absolute control mode and the current value can be read from the Absolute Value CSR. Otherwise, the Value field holds the current raw value setting.
		-----	[2 ... 4]	reserved
		One Push	[5]	If 1, a one push operation was in progress.
		ON/OFF	[6]	0: The feature was disabled, ignore the value 1: The feature was enabled
		A/M Mode	[7]	0: The feature was in manual control mode 1: The feature was in auto control mode
		--	[8 ... 19]	Reserved
		Value	[20 ... 31]	Value of the feature
4	Gain Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	[0 ... 31]	Floating point value with IEEE/real*4 format Unit: dB
8	Shutter CSR [4 bytes]	Content of the DCAM Shutter CSR Same layout as the GAIN CSR		
12	Shutter Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	[0 ... 31]	Floating point value with IEEE/real*4 format Unit: sec
16	Gamma CSR [4 bytes]	Content of the DCAM Gamma CSR Same layout as the Gain CSR		
20	Gamma Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	[0 ... 31]	Floating point value with IEEE/real*4 format Unit: dB

24	White Balance CSR [4 Bytes]	Content of the DCAM White Balance CSR		
		Field	**Bit**	**Description**
		Presence Inq	[0]	Presence of this feature If 0, the DCAM feature is not available and all of its values should be ignored
		Abs Control	[1]	Absolute control mode If 1, the DCAM feature is in absolute control mode and the current value can be read from the Absolute Value CSR. Otherwise, the Value field holds the current raw value setting.
		-----	[2 ... 4]	reserved
		One Push	[5]	If 1, a one push operation was in progress.
		ON/OFF	[6]	0: The feature was disabled, ignore the value 1: The feature was enabled
		A/M Mode	[7]	0: The feature was in manual control mode 1: The feature was in auto control mode
		Blue Value	[8 ... 19]	Blue value
		Red Value	[20 ... 31]	Red Value
28	White Balance Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	[0 ... 31]	Floating point value with IEEE/real*4 format Unit: K
32	Brightness CSR [4 bytes]	Content of the DCAM Brightness CSR Same layout as the Gain CSR		
36	Brightness Absolute Value CSR [4 Bytes]	**Field**	**Bit**	**Description**
		Abs Value	[0 ... 31]	Floating point value with IEEE/real*4 format Unit: %
40	Chunk GUID [16 Bytes]	911C8982 - 1C0F - 11D8 - 8AF0 - 00105A5BAE55		
56	Chunk Length [4 bytes]	This chunk's total length in bytes.		
60	Inverted Chunk Length [4 bytes]	The bitwise complement of the chunk length.		

6.7.5 CRC Checksum

The CRC Checksum feature adds a chunk to each image frame containing a 16 bit CRC checksum calculated using the Z-modem method. The CRC Checksum chunk is always the last chunk added to the image data stream and the chunk is always 32 bits in size. As shown in Figure 6-2, the checksum is calculated using all of the image data and all of the appended chunks except for the checksum itself.

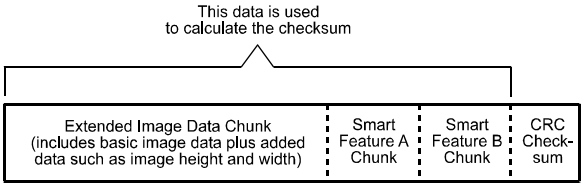

Figure 6-2: Data Used for the Checksum Calculation

The extended data stream feature (see Section 6.7.1) must be enabled in order to use the CRC Checksum feature or any of the other smart feature that adds information to the image data stream. Disabling the extended data stream feature switches off all smart features that add information to the image data stream.

The CRC Checksum feature will only work when the camera is set for video format 7.

Control and Status Register for the CRC Checksum Feature

Name	CRC Checksum	
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID	3B34004E - 1B84 - 11D8 - 83B3 - 00105A5BAE55	
Field	**Bit**	**Description**
Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
----	[1 ... 30]	Reserved
Enable (Read / write)	[31]	Enable / Disable this feature 0: Disable 1: Enable

CRC Checksum Chunk Layout

The CRC checksum is an exception to the normal chunk structure. The CRC chunk is always 32 bits wide and is always the last chunk appended to the image data. The lower 16 bits of the chunk are filled with the checksum and the upper 16 bits of the chunk are filled with zeros.

Bit	Description
[0 ... 7]	CRC Checksum low byte
[8 ... 15]	CRC Checksum high byte
[16 ... 23]	0x00
[24 ... 31]	0x00

Using the Checksum to Check the Data Integrity

When the checksum smart feature is enabled, the following two C functions can be used to check if an acquired frame contains a valid CRC checksum. The user must pass the acquired image buffer and the buffer's length in bytes to the CheckBuffer() function. The CheckBuffer() function uses the CRC16() function to calculate the checksum.

These two samples are intended to aid you in developing the code for your application. They are provided solely as examples.

```
/** \brief Calculates a 16 bit CRC checksum
  * \param pData Pointer to the data buffer
  * \param nbyLength Size of the buffer in bytes
  * \return The CRC checksum
  */
unsigned short CRC16(const unsigned char *pData, unsigned long nbyLength )
{
      unsigned long i, j, c, bit;
      unsigned long crc = 0;
      for (i=0; i<nbyLength; i++) {
            c = (unsigned long)*pData++;
            for (j=0x80; j; j>>=1) {
                  bit = crc & 0x8000;
                  crc <<= 1;
                  if (c & j) bit^= 0x8000;
                  if (bit) crc^= 0x1021;
            }
      }
      return (unsigned short) (crc & 0xffff);
}
```

```
/** \brief Verifies a frame buffer's CRC checksum
  * \param pData Pointer to the frame
  * \param nbyLength Size of frame in bytes
  * \return 1, if the check succeeds, 0 otherwise
  */
int CheckBuffer(const unsigned char* pData, unsigned long nbyLength )
{
      unsigned long nCurrentCRC, nDesiredCRC;
      /* Calculate the CRC checksum of the buffer. Don't take the last four bytes
         containing the checksum into account */
      nCurrentCRC = CRC16(pData, nbyLength - sizeof( unsigned long ) );
      /* Retrieve the desired CRC value from the data buffer */
      nDesiredCRC =  ((unsigned long*) pData)[ nbyLength / sizeof ( unsigned long ) - 1];
      /* Return TRUE if they are equal */
      return nCurrentCRC == nDesiredCRC;
}
```

6.7.6 Test Images

A102f cameras include a test image mode as a smart feature. The test image mode is used to check the camera's basic functionality and its ability to transmit an image via the video data cable. The test image mode can be used for service purposes and for failure diagnostics. In test mode, the image is generated with a software program and the camera's digital devices and does not use the optics, the CMOS pixel array, or the ADCs. Three test images are available on **A102f** cameras.

When a test image is active, the gain, brightness, and exposure time have no effect on the image.

The test image smart feature does not add information to the image data stream and can be enabled even when the extended data stream feature (see Section 6.7.1) is disabled.

The test image feature will work when the camera is set for any valid video format.

Test Image one

Test image one is designed for use with monochrome, 8 bit output modes. As shown in Figure 6-3, test image one consists of rows with several gray scale gradients ranging from 0 to 255. Assuming that the camera is operating at full 1392 x 1040 resolution and is set for a monochrome, 8 bit output mode, when the test images are generated:

- Row 0 starts with a gray value of 0 for the first pixel,
- Row 1 starts with a value of 1 for the first pixel,
- Row 2 starts with a gray vale of 2 for the first pixel, and so on.

(If the camera is operating at a lower resolution when the test images are generated, the basic appearance of the test pattern will be similar to Figure 6-3, but the starting pixel values on each row will not be as described above.)

The mathematical expression for test image one is:

Gray Value = [x + y] MOD 256

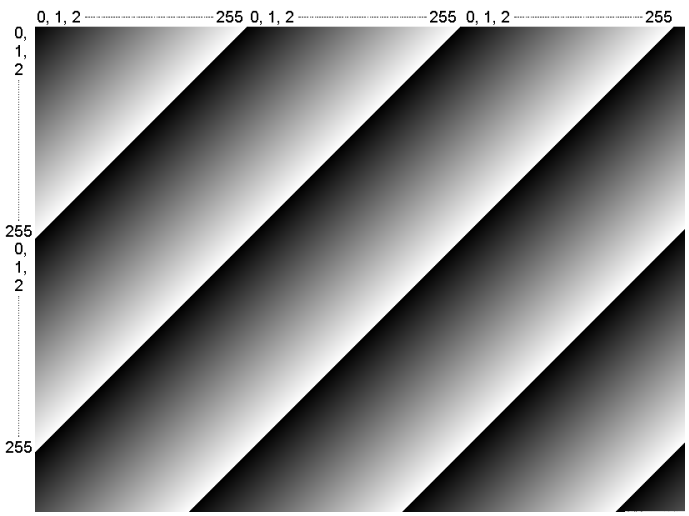

Figure 6-3: Test Image One

Test Image Two

Test image two is designed for use with monochrome, 16 bit output modes. Test image two consists of rows with several gray scale gradients ranging from 0 to 4095. Assuming that the camera is operating at full 1392 x 1040 resolution and is set for a monochrome, 16 bit output mode, when the test images are generated:

- Row 0 starts with a gray value of 0 for the first pixel, 1 for the second pixel, 2 for the third pixel, 3 for the fourth pixel, ...
- Row 1 starts with a gray value of 4 for the first pixel, 5 for the second pixel, 6 for the third pixel, 7 for the fourth pixel, ...
- Row 2 starts with a gray value of 8 for the first pixel, 9 for the second pixel, 10 for the third pixel, 11 for the fourth pixel, ...
- Row 3 starts with a gray value of 12 for the first pixel, 13 for the second pixel, 14 for the third pixel, 15 for the fourth pixel, ...

(If the camera is operating at a lower resolution when the test images are generated, the basic appearance of the test pattern will be similar to the description above, but the staring pixel values on each row will not be as described.)

The mathematical expression for test image two is:

Gray Value =[x + 4y] Mod 4096

Test image two is designed as a 16 bit test pattern. A 16 bit test pattern can not be properly displayed on standard 8 bit monitors. If you set the camera for 16 bit output and enable test pattern two, the pixel values in the test pattern will not be as described above when viewed on an 8 bit monitor.

If you set the camera for 8 bit output and enable test pattern two, the pixel values in the test pattern will not be as described above.

Test Image Three

Test image three is similar to test image one but it is not stationary. The image moves by 1 pixel from right to left whenever a one-shot or a continuous-shot command signal is sent to the camera.

Control and Status Register for the Test Image Feature

Name	Test Images	
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.	
CSR GUID	2A411342 - C0CA - 4368 - B46E - EE5DEEBF0548	
Field	**Bit**	**Description**
Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
-----	[1 ... 7]	Reserved
Image Inq 1 (Read only)	[8]	Presence of test image 1 0: Not Available 1: Available
Image Inq 2 (Read only)	[9]	Presence of test image 2 0: Not Available 1: Available
Image Inq 3 (Read only)	[10]	Presence of test image 3 0: Not Available 1: Available
Image Inq 4 (Read only)	[11]	Presence of test image 4 0: Not Available 1: Available
Image Inq 5 (Read only)	[12]	Presence of test image 5 0: Not Available 1: Available
Image Inq 6 (Read only)	[13]	Presence of test image 6 0: Not Available 1: Available
Image Inq 7 (Read only)	[14]	Presence of test image 7 0: Not Available 1: Available
-----	[15]	Reserved
Image On (Read / write)	[16 ... 18]	0: No test image active 1: Test image 1 active 2: Test image 2 active 3: Test image 3 active
-----	[19 ... 31]	Reserved

6.7.7 Extended Version Information

A102f cameras include a register that contains version numbers for the camera's internal software. For troubleshooting purposes, Basler technical support may ask you to read this register and to supply the results.

The extended version information smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The extended version feature will work when the camera is set for any valid video format.

Control and Status Register for the Extended Version Information Feature

Name	Extended Version Information	
Address	See "Determining the Address of Smart Features CSRs" on page 6-4.	
CSR GUID	2B2D8714 - C15E - 4176 - A235 - 6EF843D747B4	
Field	**Bit**	**Description**
Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
-----	[1 ... 7]	Reserved
Length	[8 ... 15]	Specifies the length in quadlets of the "string" field.
-----	[16 ... 31]	Reserved
Version Info	[n Bytes]	An ASCII character string that includes the version numbers for the camera's internal software. The length of this string field is equal to the number of quadlets given in the "length" field above.

The ASCII character string in the Version Info field contains the camera's "firmware ID" number. You can read the string to determine your camera's firmware ID. The ID number's position in the string is described in Section 1.1.

6.7.8 Lookup Table

The **A102f** camera has a sensor that reads pixel values at a 12 bit depth, however, the camera can be set to output pixel values at an 8 bit depth. When set for 8 bit output, the camera normally uses an internal process to convert the 12 bit pixel values from the sensor to the 8 bit values transmitted out of the camera. **A102f** cameras also include a smart feature that allows you to use a custom lookup table to map the 12 bit sensor output to 8 bit camera output rather than using the internal process.

The lookup table is essentially just a list of 4096 values, however, not every value is the table is actually used. If we number the values in the table from 0 through 4095, the table works like this:

- The number at location 0 in the table represents the 8 bit value that will be transmitted out of the camera when the sensor reports that a pixel has a value of 0.
- The numbers at locations 1 through 7 are not used.
- The number at location 8 in the table represents the 8 bit value that will be transmitted out of the camera when the sensor reports that a pixel has a value of 8.
- The numbers at locations 9 through 15 are not used.
- The number at location 16 in the table represents the 8 bit value that will be transmitted out of the camera when the sensor reports that a pixel has a value of 16.
- The numbers at locations 17 through 23 are not used.
- The number at location 24 in the table represents the 8 bit value that will be transmitted out of the camera when the sensor reports that a pixel has a value of 24.
- And so on.

As you can see, the table does not include an 8 bit output value for every pixel value that the sensor can report. So what does the camera do when the sensor reports a pixel value that is between two values that have a defined 8 bit output? In this case, the camera performs a straight line interpolation to determine the 8 bit value that it should transmit. For example, assume that the sensor reports a pixel value of 12. In this case, the camera would perform a straight line interpolation between the values at location 8 and location 16 in the table. The result of the interpolation would be reported out of the camera at an 8 bit depth.

Another thing to keep in mind about the table is that location 4088 is the last location that will have a usable 8 bit value associated with it. (Locations 4089 to 4095 are not used.) If the sensor reports a value above 4088, the camera will not be able to perform an interpolation. In cases where the sensor reports a value above 4088, the camera simply transmits the 8 bit value from location 4088 in the table.

Please look at page 6-25 and examine the layout of the control and status register for the lookup table smart feature. You will notice that the first two quadlets of the register include bits that allow you to check for this feature's presence and to enable or disable the feature. These initial two quadlets are followed by 4096 quadlets. The 4096 quadlets contain the values that make up the customized lookup table.

The advantage of the lookup table feature is that it allows the user to customize the response curve of the camera. The graphs below represent the contents of two typical lookup tables. The first graph is for a lookup table where the values are arranged so that the output of the camera increases linearly as the sensor output increases. The second graph is for a lookup table where the values are arranged so that the camera output increases quickly as the sensor output moves from 0 through 2048 and increases gradually as the sensor output moves from 2049 through 4096.

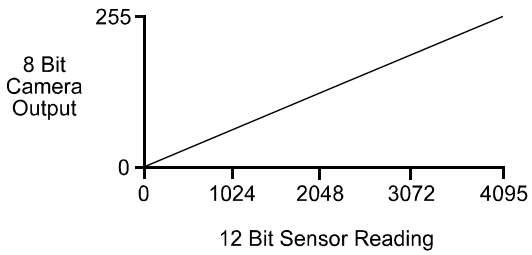

Figure 6-4: LUT with Values Mapped in a Linear Fashion

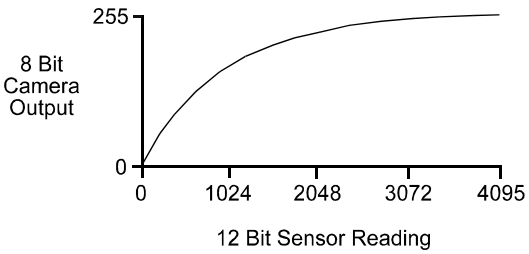

Figure 6-5: LUT with Values Mapped for Higher Camera Output at Low Sensor Readings

The lookup table smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The gain and offset functions remain active when the lookup table is used. Gain and offset are applied to the pixel values reported from the sensor **before** the pixel values are processed with the lookup table.

The lookup table feature will work when the camera is set for any valid video format.

When you enable the lookup table feature, a default lookup table is automatically loaded into the camera (see Section 6.7.9 for more information about the default table). If you want use your own customized lookup table you must:

1. Use the look table feature Control and Status Register (CSR) to enable the lookup table feature.
2. Write the values for your customized lookup table to the CSR.

Control and Status Register for the Lookup Table Feature

Name	Lookup Table		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	B28C667C - DF9D - 11D7 - 8693 - 000C6E0BD1B0		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
	-----	[1 ... 30]	Reserved
	Enable (Read / write)	[31]	Enable / Disable this feature 0: Disable 1: Enable
4	In Depth Inq (Read only)	[0 ... 15]	Bit depth of the pixel data reported by the sensor.
	Out Depth Inq (Read only)	[16 ... 31]	Bit depth of the pixel data transmitted from the camera.
8	Quadlet 0 (Read / write)	[1 Quadlet]	Defines the 8 bit value that will be transmitted from the camera when the 12 bit pixel value from the sensor is 0. (The 8 LSBs of the quadlet carry the data for the field. The 24 MSBs are all zeros.)
12 ... 36	Quadlet 1 ... 7 (Read / write)	[7 Quadlets]	Not used. The values written in these quadlets will be ignored.
40	Quadlet 8 (Read / write)	[1 Quadlet]	Defines the 8 bit value that will be transmitted from the camera when the 12 bit pixel value from the sensor is 8.
44 ... 68	Quadlet 9 ... 15 (Read / write)	[7 Quadlets]	Not used. The values written in these quadlets will be ignored.
72	Quadlet 16 (Read / write)	[1 Quadlet]	Defines the 8 bit value that will be transmitted from the camera when the 12 bit pixel value from the sensor is 16.
76 ... 100	Quadlet 17 ... 23 (Read / write)	[7 Quadlets]	Not used. The values written in these quadlets will be ignored.
104	Quadlet 24 (Read / write)	[1 Quadlet]	Defines the 8 bit value that will be transmitted from the camera when the 12 bit pixel value from the sensor is 16.
•	•	•	•
•	•	•	•
•	•	•	•
16296	Quadlet 4072 (Read / write)	[1 Quadlet]	Defines the 8 bit value that will be transmitted from the camera when the 12 bit pixel value from the sensor is 16.
16300 ... 16324	Quadlet 4073 ... 4079 (Read / write)	[7 Quadlets]	Not used. The values written here will be ignored.

16328	Quadlet 4080 (Read / write)	[1 Quadlet]	Defines the 8 bit value that will be transmitted from the camera when the 12 bit pixel value from the sensor is 4080.
16332 ... 16356	Quadlet 4081 ... 4087 (Read / write)	[7 Quadlets	Not used. The values written here will be ignored.
16360	Quadlet 4088 (Read / write)	[1 Quadlet]	Defines the 8 bit value that will be transmitted from the camera when the 12 bit pixel value from the sensor is 4088.
16364 ... 16388	Quadlet 4089 ... 4095 (Read / write)	[7 Quadlets]	Not used. The value written here will be ignored.

Using the SFF Viewer to Upload a Lookup Table

The Configurator window in the Basler SFF Viewer (see Section 6.4) includes a drop down list that can be used to enable the lookup table feature. It also includes an *Upload* button that can be used to easily load a text file containing a customized lookup table into the camera. The file must be plain text and must be formatted correctly. The file must have 4096 lines with each line containing two comma-separated values. The first value on each line represents a 12 bit pixel reading from the sensor and the second value represents the corresponding 8 bit output that will be transmitted from the camera.

Not every value in the file is actually used. Only the values in line 0, line 8, line 16, line 24, etc. are used for the lookup process. However the file **must** contain 4096 lines with two comma separated values on each line. (The values on lines 1 through 7, 9 through 15, 17 through 23, etc. must be included in the text file even though they are ignored.)

The sample below shows part of a typical text file for a lookup table. Assuming that you have enabled the lookup table feature on your camera and used the *Upload* button to load a file similar to the sample into the camera:

- If the sensor reports that a pixel has a value of 0, the camera will output a value of 0.
- If the sensor reports that a pixel has a value of 8, the camera will output a value of 1.
- If the sensor reports that a pixel has a value of 16, the camera will output a value of 3.
- If the sensor reports that a pixel has a value of 4088, the camera will output a value of 255.

```
0,0
1,0
2,0
3,0
4,0
5,0
6,0
7,0
8,1
9,1
10,1
11,1
12,1
13,1
14,1
15,1
16,3
17,3
18,3
19,3
20,3
21,3
...
4082,254
4083,254
4084,254
4085,254
4086,254
4087,254
4088,255
4089,255
4090,255
4091,255
4092,255
4093,255
4094,255
4095,255
```

Figure 6-6: Sample Text File for Use With *Upload* Button

6.7.9 Lossless Compression

The **A102f** includes a feature that allows lossless compression of the 12 bit output from the camera's sensor to 8 bit output transmitted from the camera. The basis for the lossless compression feature is a mathematical process that compresses the 12 bit output from the sensor to 8 bits by removing information characterized as noise. Because this method removes only the portion of the sensor's output that represents noise, no image information is lost and the resulting images have an extended dynamic range compared to normal 8 bit images.

Lossless compression is implemented on the **A102f** by means of a lookup table. To enable lossless compression, simply enable the lookup table feature as described in Section 6.7.8. When you enable the lookup table feature, a default table is automatically loaded into the camera. The values in the default lookup table were determined using the lossless compression technique. So if you operate the camera with the lookup feature enabled and the default table loaded, the camera will output 8 bit data via lossless compression.

6.7.10 Trigger Flag and Trigger Counter

A102f cameras include a trigger flag and trigger counter feature. The trigger counter increments by one each time an image capture is triggered regardless of whether the trigger is internal (one shot or continuous shot commands) or is external (hardware or software trigger). Triggers that occur when the camera is not ready are discarded and not counted. The trigger counter wraps to zero after 65535 is reached.

If one or more triggers has been detected since the last time the Trigger Flag field was read, the trigger flag is set to one. The flag self clears with each read access.

Writes to the Trigger Count or Trigger Flag fields are ignored.

The counter field or the flag field can be polled by your camera control software to detect the receipt of a trigger signal by the camera. The camera control software can react synchronously to each trigger signal received. By using the results of the polling to know when a trigger signal is received by the camera, you can eliminate the need for a hard wired signal from the hardware device that is issuing the trigger. Keep in mind that your degree of precision depends on your polling frequency and the 1394 bus latency.

The trigger flag and trigger counter smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The trigger flag and counter feature is always enabled regardless of the video format.

Control and Status Register for the Trigger Flag and Counter Feature

Name	Trigger Flag and Counter		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	16C31A78 - 3F75 - 11D8 - 94EC - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
	-----	[1 ... 15]	Reserved
	Trigger Count (Read only)	[16 ... 31]	The trigger counter increments by one each time an image capture is triggered. The counter is reset at power on or when an initialize command is issued.
4	-----	[0 ... 30]	Reserved
	Trigger Flag (Read only)	[31]	The flag is set to 1 by each trigger. It is cleared by a read access to this register.

6.7.11 Output Port Configuration

A102f cameras are equipped with four physical output ports designated as Output Port 0, Output Port 1, Output Port 2, and Output Port 3. The output port configuration feature can be used to change the assignment of camera output signals (such as Integrate Enabled and Trigger Ready) to the physical output ports.

As shown on pages 6-31 and 6-32, there is a control and status register (CSR) for each physical output port. The Source Select field in each register is used to assign a camera signal to the associated output port. For example, the Source Select field in the register for Output Port 0 is used to assign a camera output signal to physical output port 0.

Each physical output port can be unassigned or it can have one and only one camera output signal assigned to it.

You can assign a camera output signal to more than one physical output port. For example, the Trigger Ready signal could be assigned to both physical output port 0 and physical output port 1.

The Source Select field can also be used to designate an output port as “user set.” If an output port is designated as user set, its state can be set to high or low by using the User Setting field in the CSR for the port.

The Invert field can be used to invert the signal before it is applied to the output port and the Monitor field can be used to check the current state of the output port.

When using the output port configuration feature, you should follow this sequence:

1. Read the Presence Inq field and the Source Select Inq field for the physical port you want to work with. Determine whether the port configuration feature is available for the port and if the source for the port is selectable.
2. Use the Source Select field to select a source for the output port.
(If you select “User set” as the source, the state of the physical output port may change when you set the bits in the Source Select field. This is an artifact of the camera design.)
3. Check the Monitor Inq, Invert Inq, and User Setting Inq fields. The state of these fields will tell you if the Monitor, Invert, and User Setting fields are available. (The availability of the Monitor, Invert, and User Setting fields will vary depending on the selected source.)
4. If the Invert field is available, set the field as desired.
5. If you selected “User set” as the source, use the User Setting field to set the state of the output as desired.
6. If the Monitor field is available, use the field as desired to check the current state of the output.

The output port configuration smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The output port configuration feature is always enabled regardless of the video format.

By default, the Integrate Enabled signal is assigned to physical output port 0 and the Trigger Ready Signal is assigned to physical output port 1.

Control and Status Registers for the Output Port Configuration Feature

Name	Output Port 0 Configuration		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	5A889D7E - 41E5 - 11D8 - 845B - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	[0]	Presence of the output port 0 configuration feature 0: Not Available 1: Available
	Monitor Inq (Read only)	[1]	Presence of the monitor field 0: Not Available 1: Available
	Invert Inq (Read only)	[2]	Presence of the invert field 0: Not Available 1: Available
	User Setting Inq (Read only)	[3]	Presence of the user setting field 0: Not Available 1: Available
	-----	[4 ... 26]	Reserved
	Source Select (Read / write)	[27 ... 31]	Sets the source signal for output port 0: 0: Integrate Enabled signal 1: Trigger Ready signal 3: User set (state can be set with the User Setting field described below) 4: Strobe
4	Source Select Inq (Read only)	[0 ... 31]	If bit *n* is set, then value *n* is valid for use in the Source Select field. For example, if bit 0 is set, then 0 is a valid value for use in the Source Select field. If bit 1 is set, then 1 is a valid value for use in the Source Select field. Etc.
8	-----	[0 ... 30]	Reserved
	Monitor (Read only)	[31]	Shows the current state of the output: 0: Low (non-conducting) 1: High (conducting)
12	-----	[0 ... 30]	Reserved
	Invert (Read / write)	[31]	Enables signal inversion: 0: Do not invert 1: Invert
16	-----	[0 ... 30]	Reserved
	User Setting (Read / write)	[31]	If the Source Select field is set to “user set”, this field sets the state of the output: 0: Low (non-conducting) 1: High (conducting) (Sets the state of the output **before** the inverter.)
20	-----	[0 ... 31]	Reserved

Name	Output Port 1 Configuration		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	949D820A - 4513 - 11D8 - 9EB1 - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Same as port 0.		
4	Same as port 0.		
8	Same as port 0.		
12	Same as port 0.		
16	Same as port 0.		
20	Same as port 0.		

Name	Output Port 2 Configuration		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	C14E5072 - 4513 - 11D8 - 81F3 - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Same as port 0.		
4	Same as port 0.		
8	Same as port 0.		
12	Same as port 0.		
16	Same as port 0.		
20	Same as port 0.		

Name	Output Port 3 Configuration		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	E79233CA - 4513 - 11D8 - 9B9A - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Same as port 0.		
4	Same as port 0.		
8	Same as port 0.		
12	Same as port 0.		
16	Same as port 0.		
20	Same as port 0.		

6.7.12 Startup Memory Channel

As described in Section 3.15, **A102f** cameras include four memory channels that can be used to store camera configuration sets. Memory channel 0 contains a factory configuration set. Channels 1, 2 and 3 can be used to store user created configuration sets. The startup memory channel smart feature lets you designate a memory channel and when the camera is powered on or reset, the contents of the designated channel will be copied into the work set in the camera's volatile memory.

To designate a startup memory channel, write a value to the Channel field of the Startup Memory Channel CSR.

You can only designate memory channel 1, 2 or 3 as the startup chanel if you have previously saved a configuration set into the designated channel. You cannot use an empty memory channel as the startup channel. See Section 3.15.

The startup memory channel smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The startup memory channel smart feature is always enabled regardless of the video format.

Control and Status Register for the Startup Memory Channel Feature

Name	Startup Memory Channel		
Address	See "Determining the Address of Smart Features CSRs" on page 6-4.		
CSR GUID	93A06C5C - 87BF - 11D8 - 86DD - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	[0]	Presence of this feature 0: Not Available 1: Available
	-----	[1 ... 27]	Reserved
	Channel	[28 ... 31]	Selects a memory channel. At camera power on or reset, the selected channel will be copied into the camera's work configuration set. 0: Channel 0 (Factory set) 1: Channel1 2: Channel 2 3: Channel 3 Default = 0

6.7.13 Shutter Time Base

As described in Section 3.2.1, exposure time is determined by a combination of two values. The first is the setting in the Value field of the Shutter control register (see page 4-22). The second is the Shutter Time Base. Exposure time is determined by the product of these two values:

Exposure Time = (Shutter Value Setting) x (Shutter Time Base)

The shutter time base is fixed at 20 µs by default and the exposure time is normally adjusted by changing the setting in the Value field of the Shutter control register. However, if you require an exposure time that is shorter or longer than what you can achieve by changing the shutter value alone, the Shutter Time Base CSR can be used to change the shutter time base.

To change the shutter time base:

- Set the Enable field in the Shutter Time Base CSR to 1
- Set the Time Base field to your desired time base value

Example

Assume that you have set the Value field of the Shutter control register to 325. Also assume that you have enabled the time base smart feature and that you have set the Time Base field in the Shutter Time Base CSR to 0.000150 second. In this case:

Exposure Time = (Shutter Value Setting) x (Shutter Time Base)

Exposure Time = (325) x (0.000150 s)

Exposure Time = 0.048750 s

The shutter time base smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The shutter time base smart feature can be enabled regardless of the video format.

Control and Status Register for the Shutter Time Base Feature

Name	Shutter Time Base		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	648BE1DA - A416 - 11D8 - 9B47 - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	[0]	Presence of the shutter time base feature 0: Not Available 1: Available
	-----	[1 ... 30]	Reserved
	Enable (Read / write)	[31]	Enable / Disable this feature 0: Disable 1: Enable
4	Increment (Read only)	[0 ... 31]	Increment (in seconds) by which the time base field can be adjusted. The value in the increment field is a standard IEEE-754 single precision (32 bit) floating point number.
8	Min (Read only)	[0 ... 31]	Minimum value (in seconds) for the time base field. The value in the min field is a standard IEEE-754 single precision (32 bit) floating point number.
12	Min (Read only)	[0 ... 31]	Maximum value (in seconds) for the time base field. The value in the max field is a standard IEEE-754 single precision (32 bit) floating point number.
16	Time Base (Read / write)	[0 ... 31]	Sets the shutter time base in seconds. The time base can range from 0.000015 second to 0.001221 second in increments of 0.000001 second. The value in the time base field is a standard IEEE-754 single precision (32 bit) floating point number. Default = 0.000020 second

6.7.14 Strobe Time Base

The strobe time base smart feature can be used to change the delay time base and the duration time base for the strobe control feature (see Section 3.10).

Changing the Strobe Delay Time Base

As described in Section 3.10, the delay for any one of the strobe signals is determined by a combination of two values. The first is the setting in the Delay Value field of the corresponding Strobe Control register (see page 4-22). The second is the Strobe Delay Time Base. For example, the Strobe 0 delay will be determined by the product of these two parameters:

Strobe 0 Delay = (Strobe 0 Delay Value Setting) x (Strobe Delay Time Base)

The strobe delay time base is fixed at 1/1024 ms by default and the strobe delay time is normally adjusted by changing the setting in the Delay Value field of the corresponding Strobe Control register. However, if you require a delay that is longer than what you can achieve by changing the strobe delay value alone, the Strobe Time Base CSR can be used to change the strobe delay time base.

To change the strobe delay time base:

- Set the Delay Time Base field in the Strobe Time Base CSR to your desired time base value

Example

Assume that you have set the Delay Value field of the Strobe 0 control register to 186. Also assume that you have set the Delay Time Base field in the Strobe Time Base CSR to 14. In this case:

Strobe 0 Delay = (Strobe 0 Delay Value Setting) x (Strobe Delay Time Base)

Strobe 0 Delay = (186) x (14/1024 ms)

Strobe 0 Delay = 2.54 ms

Changing the Strobe Duration Time Base

As described in Section 3.10, the duration for any one of the strobe signals is determined by a combination of two values. The first is the setting in the Duration Value field of the corresponding Strobe Control register (see page 4-22). The second is the Strobe Duration Time Base. For example, the Strobe 0 duration will be determined by the product of these two parameters:

Strobe 0 Duration = (Strobe 0 Duration Value Setting) x (Strobe Duration Time Base)

The strobe duration time base is fixed at 1/1024 ms by default and the strobe duration is normally adjusted by changing the setting in the Duration Value field of the corresponding Strobe Control register. However, if you require a duration that is longer than what you can achieve by changing the strobe duration value alone, the Strobe Time Base CSR can be used to change the strobe duration time base.

To change the strobe duration time base:

- Set the Duration Time Base field in the Strobe Time Base CSR to your desired time base value

Example

Assume that you have set the Duration Value field of the Strobe 0 control register to 423. Also assume that you have set the Duration Time Base field in the Strobe Time Base CSR to 5. In this case:

Strobe 0 Duration = (Strobe 0 Duration Value Setting) x (Strobe Duration Time Base)

Strobe 0 Duration = (423) x (5/1024 ms)

Strobe 0 Duration = 2.07 ms

There is only one setting for the strobe delay time base and this single setting is used by all four of the available strobe outputs.

There is only one setting for the strobe duration time base and this single setting is used by all four of the available strobe outputs.

The strobe time base smart feature does not add information to the image data stream and can be accessed even when the extended data stream feature (see Section 6.7.1) is disabled.

The strobe time base smart feature can be enabled regardless of the video format.

Control and Status Register for the Strobe Time Base Feature

Name	Strobe Time Base		
Address	See “Determining the Address of Smart Features CSRs” on page 6-4.		
CSR GUID	E77E6336 - E617 - 11D8 - 9653 - 00105A5BAE55		
Position	**Field**	**Bit**	**Description**
0	Presence Inq (Read only)	[0]	Presence of the shutter time base feature 0: Not Available 1: Available
	-----	[1 ... 15]	Reserved
	Duration Time Base (Read / write)	[16 ... 23]	The value in this field is an integer value and can range between 1 and 85. The value sets the duration time base in units of 1/1024 ms. Example: If the value in this field is set to 14, the duration time base will be 14/1024 ms (~ 13.7 µs) Default = 1
	Delay Time Base (Read only)	[24 ... 31]	The value in this field is an integer value and can range between 1 and 85. The value sets the delay time base in units of 1/1024 ms. Example: If the value in this field is set to 14, the delay time base will be 14/1024 ms (~ 13.7 µs) Default = 1

6.8 Customized Smart Features

The Basler **A102f** has significant processing capabilities and Basler can accommodate customer requests for customized smart features. A great advantage of the smart features framework is that it serves as a standardized platform for parameterizing any customized smart feature and for returning the results from the feature.

The Basler camera development team is ready and able to handle requests for customized smart features. The cost to the customer for adding a customized smart feature to the **A102f** will depend on the complexity of algorithm, software, and firmware development, of incorporating the feature within the smart features framework, and of testing to ensure that the feature meets specifications. Please contact your Basler sales representative for more details about customized smart features.

7 Mechanical Considerations

The **A102f** camera housing is manufactured with high precision. Planar, parallel, and angular sides guarantee precise mounting with high repeatability.

Caution!

The camera is shipped with a cap on the lens mount. To avoid collecting dust on the sensor, make sure that at all times either the cap is in place or a lens is mounted on the camera.

7.1 Camera Dimensions and Mounting Facilities

The dimensions for **A102f** cameras are as shown in Figure 7-1.

A102f cameras are equipped with four M4 mounting holes on the front and two M4 mounting holes on each side as indicated in the drawings.

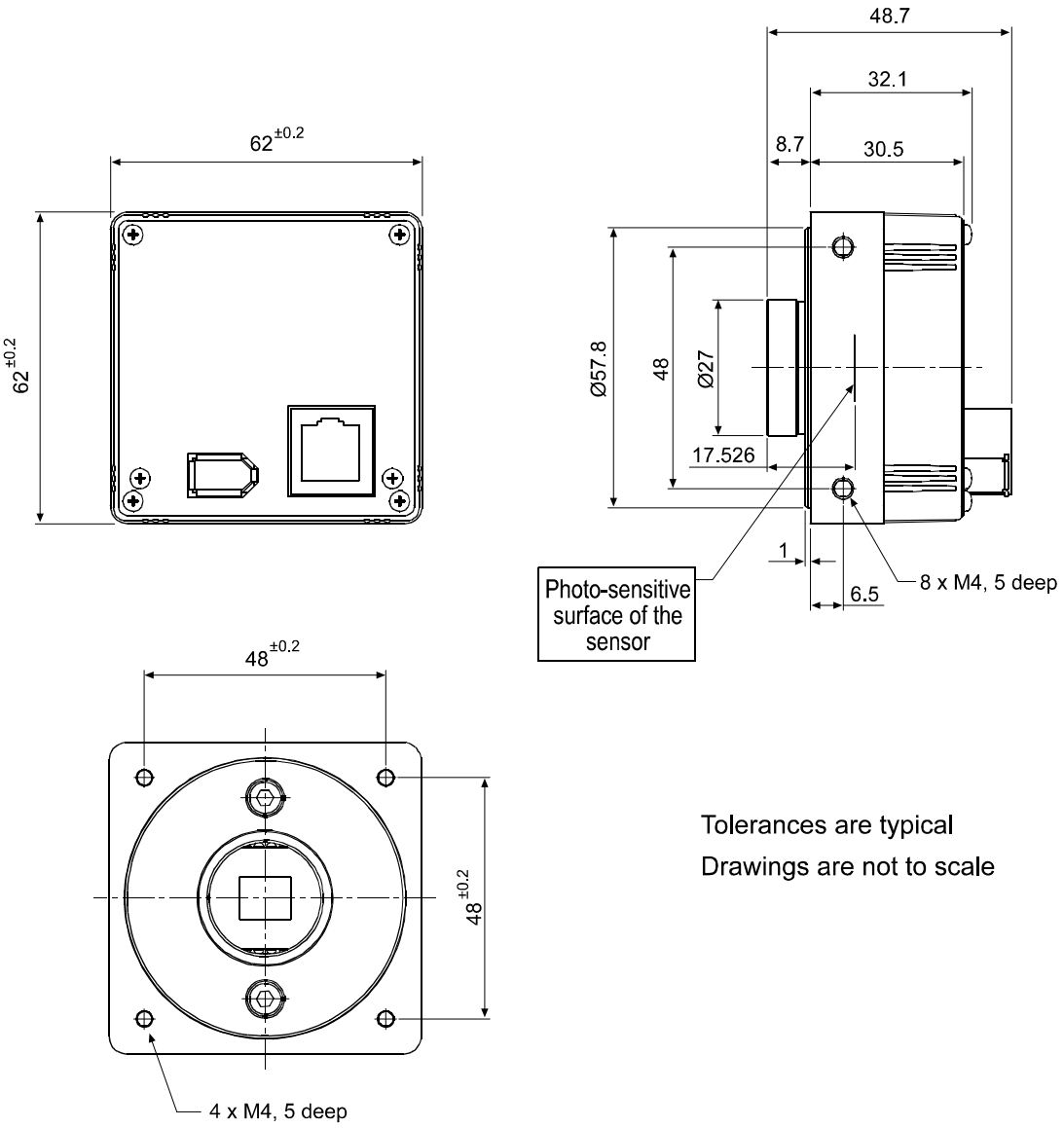

Figure 7-1: **A102f** Mechanical Dimensions (in mm)

7.2 Sensor Positioning Accuracy

The sensor positioning accuracy in the horizontal and vertical directions is as shown in Figure 7-2. Rotational accuracy is also shown in the figure.

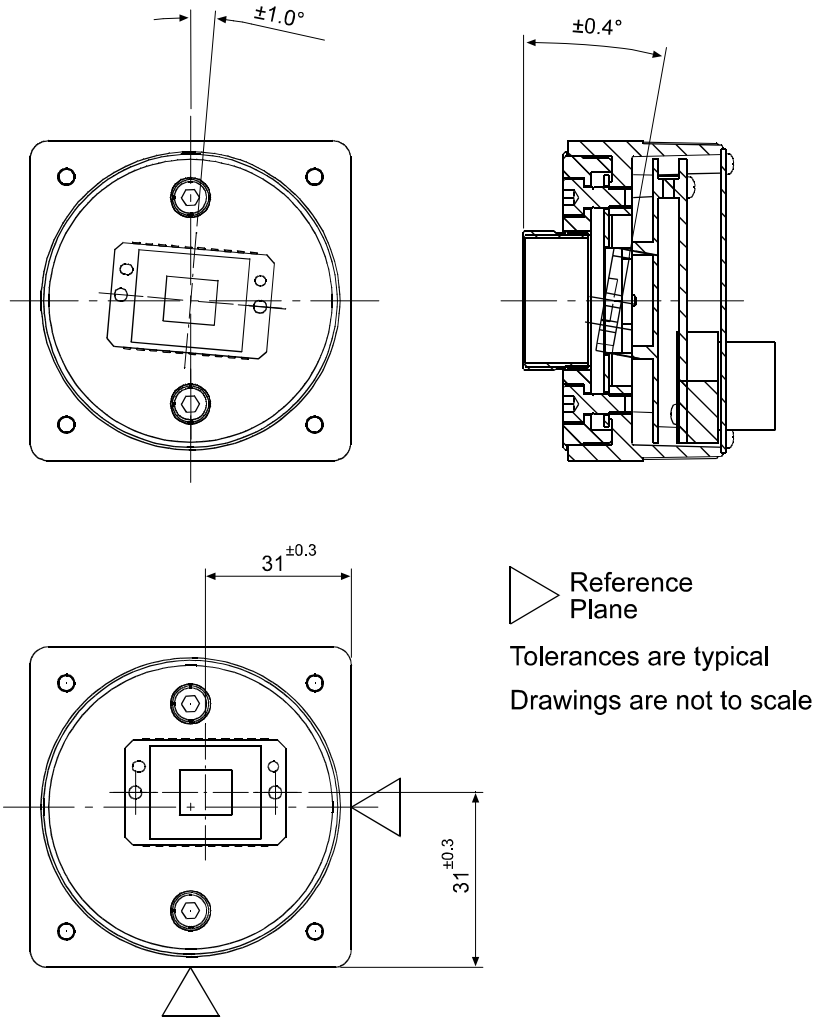

Figure 7-2: Sensor Positioning Accuracy

7.3 Maximum Lens Thread Length on the A102fc

A102fc cameras are normally equipped with a C-mount lens adapter that contains an internal IR cut filter. As shown in Figure 7-3, the thread length of the C-mount lens must used on the camera must be less than 7.5 mm. If a lens with a longer thread length is used, the IR cut filter will be damaged or destroyed and the camera will no longer operate.

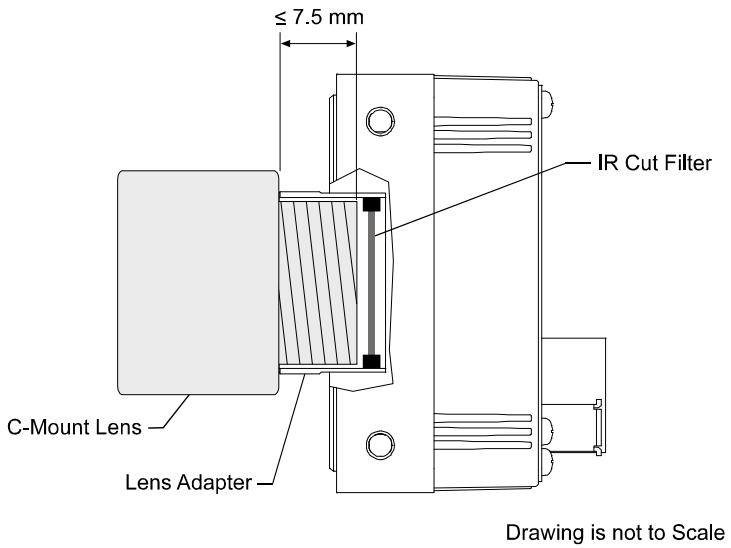

Figure 7-3: Maximum Lens Thread Length on A102fc Cameras

Caution!

A102fc color cameras are equipped with an IR cut filter mounted in of the lens adapter. The location of the filter limits the thread length of the lens that can be used on the camera. The thread length on your lens must be less than 7.5 mm. If a lens with a longer thread length is used, the camera will be damaged and will no longer operate.

7.4 Mechanical Stress Test Results

The **A102f** was submitted to an independent mechanical testing laboratory and subjected to the stress tests listed below. After mechanical testing, the camera exhibited no detectable physical damage and produced normal images during standard operational testing.

Test	Standard	Conditions
Vibration (each axis)	IEC 60068-2-6	10-58 Hz / 1.5 mm_58-500 Hz / 20 g_1 Octave/Minute 10 repetitions
Shock (each axis)	IEC 60068-2-27	20 g / 11 ms / 10 shocks positive 20 g / 11 ms / 10 shocks negative
Bump (each axis)	IEC 60068-2-29	20 g / 11 ms / 100 shocks positive 20 g / 11 ms / 100 shocks negative

Table 7-1: Mechanical Tests

Revision History

Doc. ID Number	Date	Changes
DA00063001	24 October 2003	Initial release of this document.
DA00063002	25 February 2004	Second draft for revision two of the manual. Added Section 1.1 describing document applicability. Updated Sections 2.5, 3.2.5, 3.3, and 3.4 to reflect the new input and output port configuration options. Added Section 3.2.4 describing the new software trigger feature. Updated the numbers in Figure 3-6 to reflect minor changes in the exposure timing. Updated the note box on page 3-20 to show restrictions when setting the AOI on color cameras. Added Section 3.6.1 describing changing the AOI on-the-fly. Updated the description of the color filter ID in Section 3.8.2. Added Section 3.9.2 regarding bit depth selection on color cameras. Added Sections 3.10 and 3.11 describing the new Strobe Control Output Signal and Parallel IO Control features. Added the Raw 16 color ID description on page 3-36. Updated the register descriptions in Section 4.4 to reflect new and revised features. Added Section 6 describing the new smart features capabilities. Revised Figure 7-1 to reflect a minor dimension change.
DA00063003	22 March 2004	Corrected errors in the description of the Control and Status Registers for PIO Control on page 4-41. Corrected errors in the description of the Control and Status Registers for the Output Port Configuration smart feature on page 6-31.
DA00063004	31 August 2004	Added a note in Section 3.2.1 indicating that 38 µs is no longer added to the exposure time. Made changes to the formula in Section 3.7 to reflect some small timing changes that were made to the camera. Updated Section 3.8.1 to describe the new method that is used for white balancing. Added a description of the new error flags in Section 3.14. Added register descriptions in Section 4.4.2 for the new error flags. Updated the drawings in Section 7.2. Added mechanical stress test results in Section 7.4.

Doc. ID Number	Date	Changes
DA00063005	2 March 2005	Added Sections 2.5.3 and 2.5.4 showing typical input circuit and typical output circuit digrams. Added Section 3.2.7 to clarify the terminology used to describe frame readout, buffering and transmission. Updated the YUV formulas in Section 3.8. Reworded the white balance and color filter ID descriptions in Sections 3.8.1 and 3.8.2 for better clarity. Added information about the new strobe time base feature to Sections 3.10 and 6.7.14. Added information about the new configuration sets and memory channels to Sections 3.15, 4.4 and 6.7.12. Reformatted and expanded the register descriptions in Section 4.4. Added Section 5 describing image data formats and structures. Corrected the CSR GUID for Output Port 3 configuration on page 6-32.
DA00063006	7 Dec 2010	Updated the European, American, and Asian contact addresses. Added Section 1.7 describing how to obtain an RMA number. Added the PS2805C-4 optocoupler in Figure 2-3. Corrected the bit assignment for the memory save channel register on page 4-18. Removed the link related to downloading the SFF software from Section 6.4. Removed the feedback page.

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